An Acoustic Charge Transport Imager for High Definition Television Applications

NASA Grant #NAGW-2753

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September, 1993

GEORGIA INSTITUTE OF TECHNOLOGY
A Unit of the University System of Georgia
Atlanta, Georgia 30332

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1.0 Highlights

The most important achievements during the past year on the ACT imager project are as follows:

1) invention of a new, ultra-low noise, low operating voltage APD which is expected to offer far better performance than the existing volume doped APD device.

2) performance of a comprehensive series of experiments on the acoustic and piezoelectric properties of ZnO films sputtered on GaAs which can possibly lead to a decrease in the required rf drive power for ACT devices by 15dB.

3) development of an advanced, hydrodynamic, macroscopic simulator used for evaluating the performance of ACT and CTD devices and aiding in the development of the next generation of devices.

4) experimental development of CTD devices which utilize a p-doped top barrier demonstrating charge storage capacity and low leakage currents.

5) refinements in materials growth techniques and insitu controls to lower surface defect densities to record levels as well as increase material uniformity and quality.

Other important milestones in the project are listed below:

1. Development of a new first principles theory of interband impact ionization which is incorporated into our microscopic, ensemble Monte Carlo simulator for APD device simulation. This offers far greater accuracy in determining APD device performance.

2. Development of technical ties to Los Alamos National Laboratory to explore ways in which our Monte Carlo and hydrodynamic simulators can be ported onto the CM5 massively parallel computer.

3. Experimental demonstration of an AlGaAs/GaAs HACT device operating at a clock frequency of 188.5 MHz with a charge transfer efficiency > 0.992 for a 1.2 cm long structure.

4. Design and construction of a novel wafer holding platform for MBE system to circumvent indium mounting.

5. Development of technical ties to Sandia National Laboratory to explore improvements in ion implantation technology related to CTD development.

6. Contractual agreements between Bell Northern Research (BNR) and Drs. Brennan and Hunt's groups to develop new APDs and HACT devices respectively have been made.

7. BNR has sent a professional employee, Mr. Tom Cameron, to work towards his Ph.D. degree with Dr. Hunt at Georgia Tech.

8. Development and testing of stack matrix theory for modeling acoustic wave propagation in multilayered structures.

9. Transfer of stack matrix theory computer design tool to various industries including BNR, SAWTEK, RF Monolithics, and Siemens.

10. Development of yield model for HACT devices.

11. Initiation of manufacturing studies including study of lifetime and failure mechanisms.

12. Identification of doping variations in APDs and development of gas source doping methodology during MBE growth to address this problem.

13. Development of automated nondestructive optical characterization system for in-line material and process control/monitoring.

14. Development of nondestructive measurement techniques for monitoring the uniformity

of HACT, CTD and APD material structure parameters and quality, as well as APD performance.

15. Statistical process control in CTD and HACT fabrication to optimize device uniformity.
16. Optimized HACT ohmic contact process for minimum contact resistance.
17. Condensed HACT mask set from five to three masks.
18. Used noncontact sheet resistivity uniformity measurements to screen starting wafers.

2.0 Objective and Approach of the Project

The primary goal of this research is to develop a solid-state high definition television (HDTV) imager chip operating at a frame rate of about 170 frames/sec, at 2 Megapixels /frame. This imager will offer an order of magnitude improvement in speed over CCD designs and will allow for monolithic imagers from the IR to UV.

From a personnel perspective, the approach has been to assemble a highly skilled team of experts in each of the attendant GaAs technologies from which the camera project derives. In addition to those involved in this project at Georgia Tech, strong collaborations with Bell Northern Research (BNR), Motorola and the National Research Council of Canada have been developed and collaborations with Los Alamos and Sandia National Labs are being pursued. Through the efforts of the team members, progress has been made towards solving many of the key issues to develop a manufacturable HDTV camera chip and hence some of the problems faced by the GaAs device industry as a whole.

The technical approach of the project focuses on the development of the three basic components of the imager and their subsequent integration. The camera chip can be

decomposed into three distinct functions: 1) image capture via an array of avalanche photodiodes (APDs) 2) charge collection, storage and overflow control via a charge transfer transitor device (CTD) and 3) charge readout via an array of acoustic charge transport (ACT) channels. The use of APDs allows for optical gain at low noise and low operating voltage while the ACT readout enables concomittant high speed and high charge transfer efficiency. Currently work is progressing towards the optimization of each of these component devices.

In addition to the development of each of the three distinct components, work towards their integration and manufacturability is also progressing. The component designs are considered not only to meet individual specifications but to provide overall system level performance suitable for HDTV operation upon integration. The ultimate manufacturability and reliability of the chip constrains the design as well.

The actual methodology of the technical approach can be summarized using Figure 2.1. The project consists of four main thrusts. Each of these thrusts is represented by a box in Figure 2.1. The first box, simulation and design, incorporates the theoretical modeling of the component devices and overall system. Simulation models are used to design, evaluate and optimize each of the system components and evaluate how each component interacts with the others. Several different simulators have been developed and their features are described in the next section. The simulation results are used to direct the actual growth and fabrication of each device which is represented by the second box in Figure 2.1. Once the devices have been fabricated, they are characterized and tested to determine their performance. This is accomplished in the third box in Figure 2.1. Finally, the device designs are evaluated as to their manufacturability and reliability. The results of the experimental investigations and

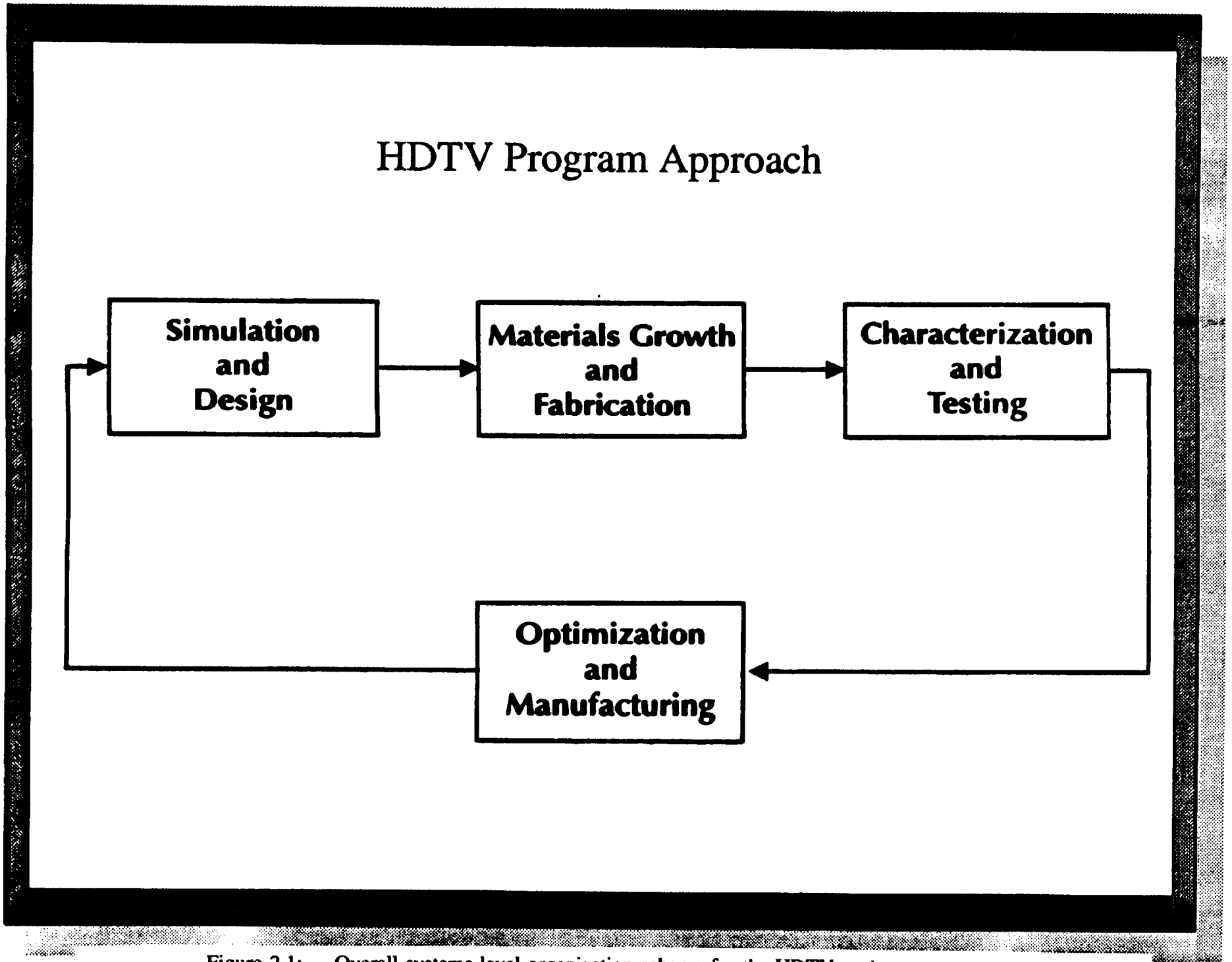


Figure 2.1: Overall systems level organization scheme for the HDTV project.

manufacturability examination serve as feedback to the design stage. Using this feedback loop, and successive iterations, a robust design of each of the device components and their successful integration can be insured.

3.0 Progress

In this section, progress during the past year of the program will be reviewed. Progress within each of the four basic thrusts of the program will be presented.

3.1 Simulation and Design

The overall simulation and design methodology is schematically presented in Figure 3.1.1. As can be seen from Figure 3.1.1, there exists two main modeling tools, one microscopic and the other macroscopic. The microscopic model is based on the ensemble Monte Carlo method. In the ensemble Monte Carlo model, the microscopic histories of the carriers are tracked in both k and real space subject to the conditions of the band structure, phonon and carrier scatterings, and the action of the applied electric fields and device boundaries. The model includes the full details of the band structures and scattering rates which are derived numerically using the fundamental physical parameters which characterize the host material. Additionally, the Monte Carlo model contains a highly advanced treatment of the impact ionization transition rate formulation. As such the Monte Carlo model provides a highly accurate, fundamentally based calculation of the carrier ionization rates in both bulk material and device structures. The Monte Carlo model can be used either to model the devices directly, (here we choose only to model the avalanche photodiodes, APDs, using the

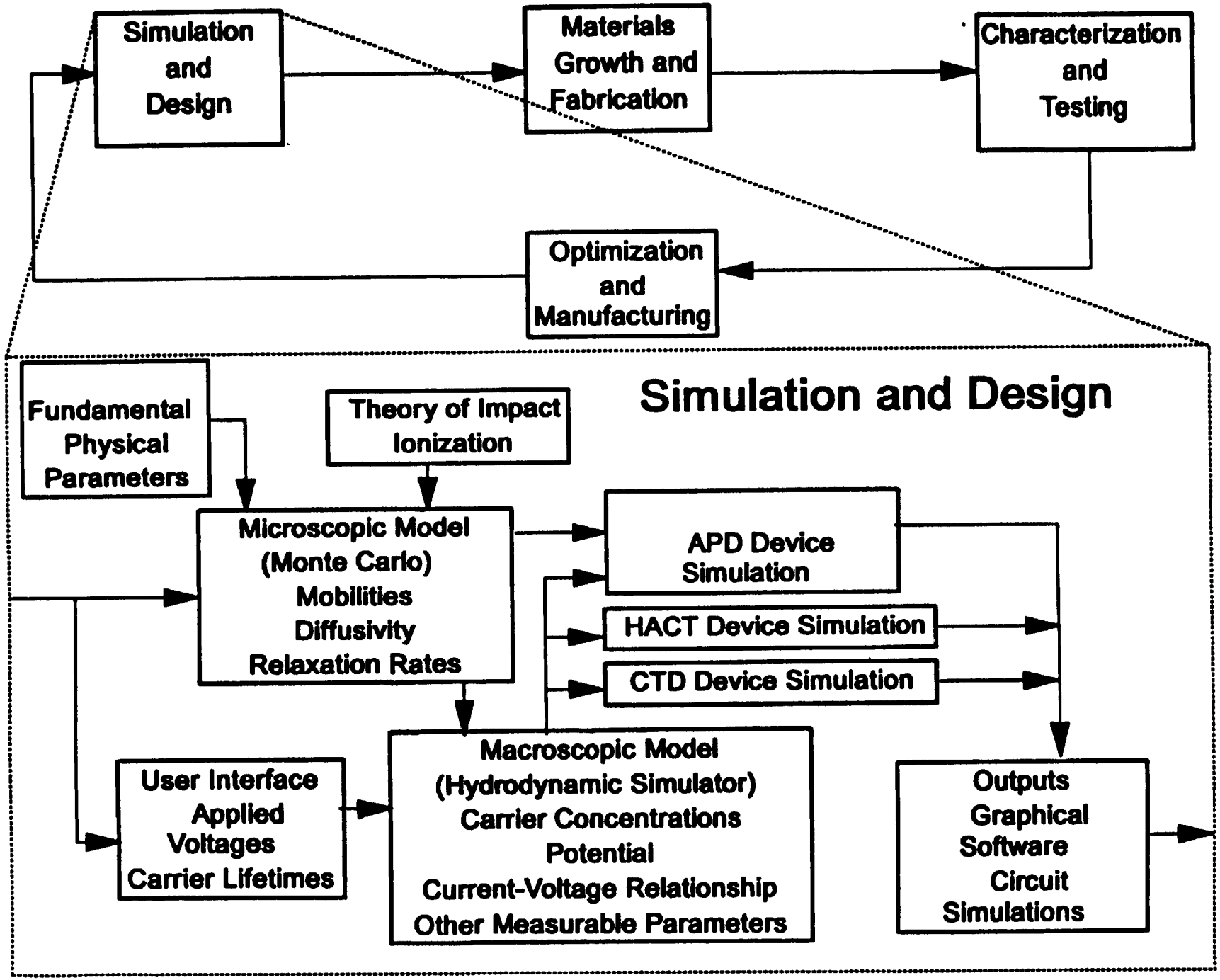


Figure 3.1.1: Detailed organization plan of the simulation and design stage.

Monte Carlo technique), or to determine many of the parameters used in the macroscopic model. As we will discuss below, the Monte Carlo method can be used to determine the energy dependent carrier mobilities and diffusivities for use in the macroscopic simulator. The details of the work performed using the Monte Carlo model are reviewed below in Section 3.1.1.

The macroscopic model used is based on a hydrodynamic solution of the transport equations. In the hydrodynamic model a series of coupled partial differential equations are solved simultaneously. These equations are derived by taking moments of the Boltzmann equation. The resulting equations that are solved are the electron and hole continuity equations, energy balance equations, flux and energy flux equations and the Poisson equation. The inputs to the macroscopic model are parameters such as the carrier mobilities, diffusivities, recombination-generation lifetimes, applied voltages, device geometry, and relaxation rates. The input parameters are typically obtained either from the Monte Carlo or if available, from experiment. Therefore, the microscopic, fundamental Monte Carlo model is used to parametrize the hydrodynamic model which is shown schematically in Figure 3.1.1. The principal advantage of the macroscopic model is that it readily provides the key engineering figures of merit needed to characterize the workings of the device among which are the current-voltage characteristic, noise, gain, capacitance-voltage characteristic, and other measurable parameters. As such, the hydrodynamic model serves as an extremely useful engineering design tool since it readily links the theory to experiment. During the course of the past year, we have developed a full hydrodynamic model and have applied it to the study of the component devices, specifically CTDs and HACTs. These details are

reviewed below in Section 3.1.2.

In addition to the microscopic and macroscopic models described above, we have developed additional design tools for studying and optimizing the HACT performance. These tools include a program to predict the electric potential propagating with a surface acoustic wave (SAW) in a multilayered material and a program to predict the waveguiding of the SAW by the HDTV imager structure (see section 3.1.3). In addition, a physically-based simulation tool for HACT devices has been developed and is resident in an RF industry-standard software environment. This approach will allow the designer to go directly from device simulation to mask layout and can be easily ported to our industrial partners (see section 3.1.4).

3.1.1 Theory of Impact Ionization and Modeling of APDs

As described above, we have applied our ensemble Monte Carlo models to the study of APDs. In order to develop an accurate assessment of APD performance, it is necessary to include a detailed description of the impact ionization transition rate in the Monte Carlo model. We have developed a new approach which includes the k-dependence of the impact ionization transition rate. The transition rate is determined using Fermi's golden rule from a two-body screened Coulomb interaction assuming energy and momentum conservation [1,2]. The transition rate is calculated for the first two conduction bands for a series of points within the reduced zone of the first Brillouin zone. The rate at each point is evaluated by numerically integrating over the final density of states within the full Brillouin zone using a k o p calculation to determine the overlap integrals. Initially, we have confined our

investigation to bulk silicon since the impact ionization rate has been extensively studied experimentally in this material. Our calculations reveal that the ionization transition rate is highly dependent on the initiating electron k-vector and that the transition rate in bulk silicon is greatest for electrons originating from within the second conduction band as can be seen from inspection of Figures 3.1.2 and 3.1.3. Inclusion of the k-dependent theory into the ensemble Monte Carlo simulator enables a highly accurate determination of the total electron impact ionization rate. The overall ionization rate in bulk silicon has been calculated using this approach. The calculated results along with representative experimental data are shown in Figure 3.1.4. Though other experimental data exist, these data comprise a representative set which bracket the range of reported experimental measurements. As can be seen from Figure 3.1.4, the k-dependent calculations match best to the low range of the experimental data [3]. Our results indicate that the ionization rate is best modeled as a soft threshold process which is in good agreement with recent theoretical studies [4]. Inclusion of this new method within our ensemble Monte Carlo APD simulator will enable a far more accurate treatment of the ionization rate and provide greater accuracy in assessing APD device performance.

The Monte Carlo simulator has been used to study alternative APD devices. Previous work [5-7] has shown that a multiquantum well APD using built-in p-i-n junctions within each stage can exhibit ultra-low noise performance. However, the low noise performance begins to deteriorate as the gain increases to values greater than 5 in these devices. We believe that the increase in the noise arises from the failure to fully deplete the built-in junctions within the devices. As a result, the applied voltage appears as a residual bias field

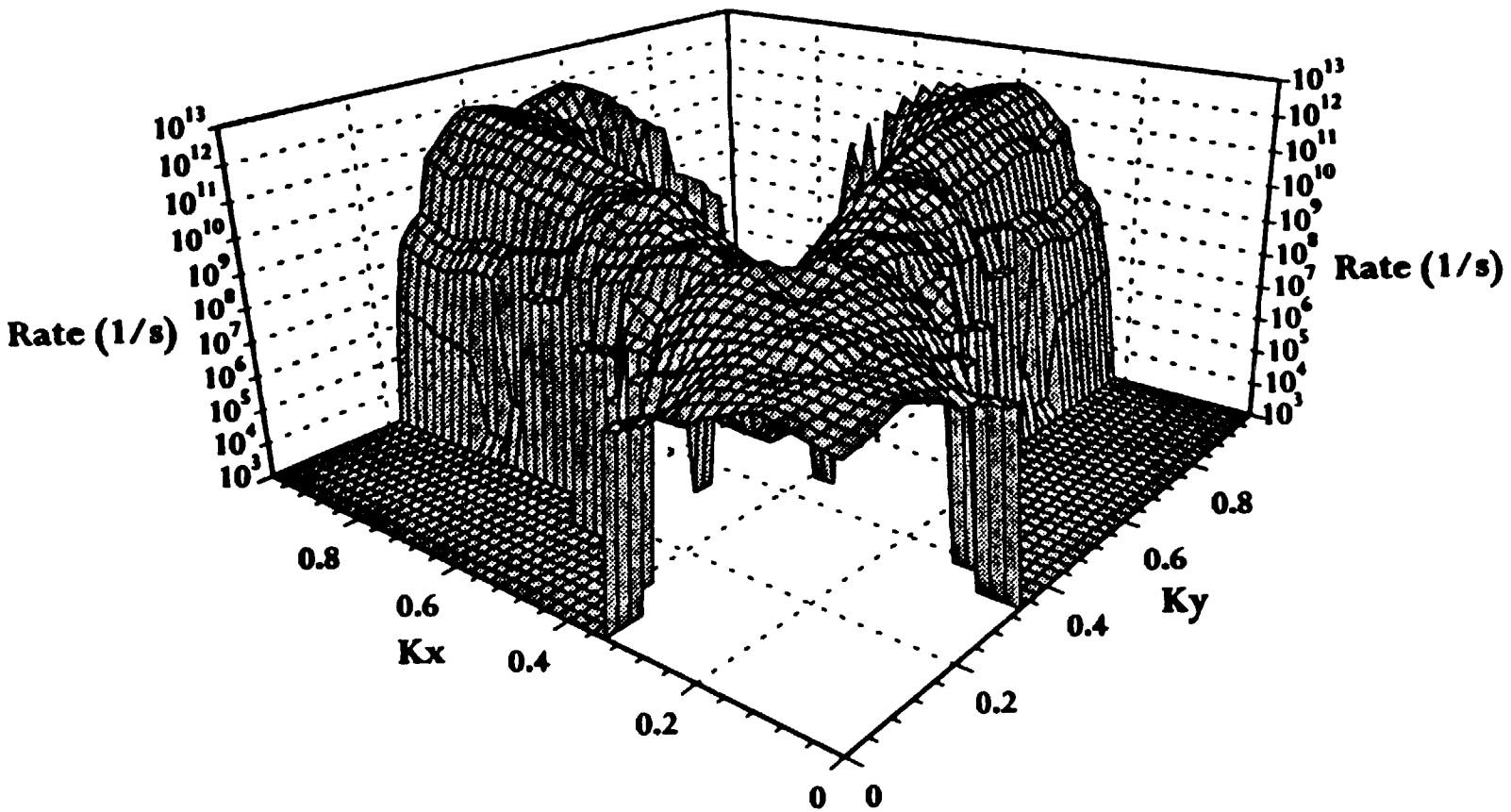


Figure 3.1.2: Impact ionization transition rate as a function of k_x, and k_y at fixed k_z=0.0 for the first conduction band of bulk silicon.

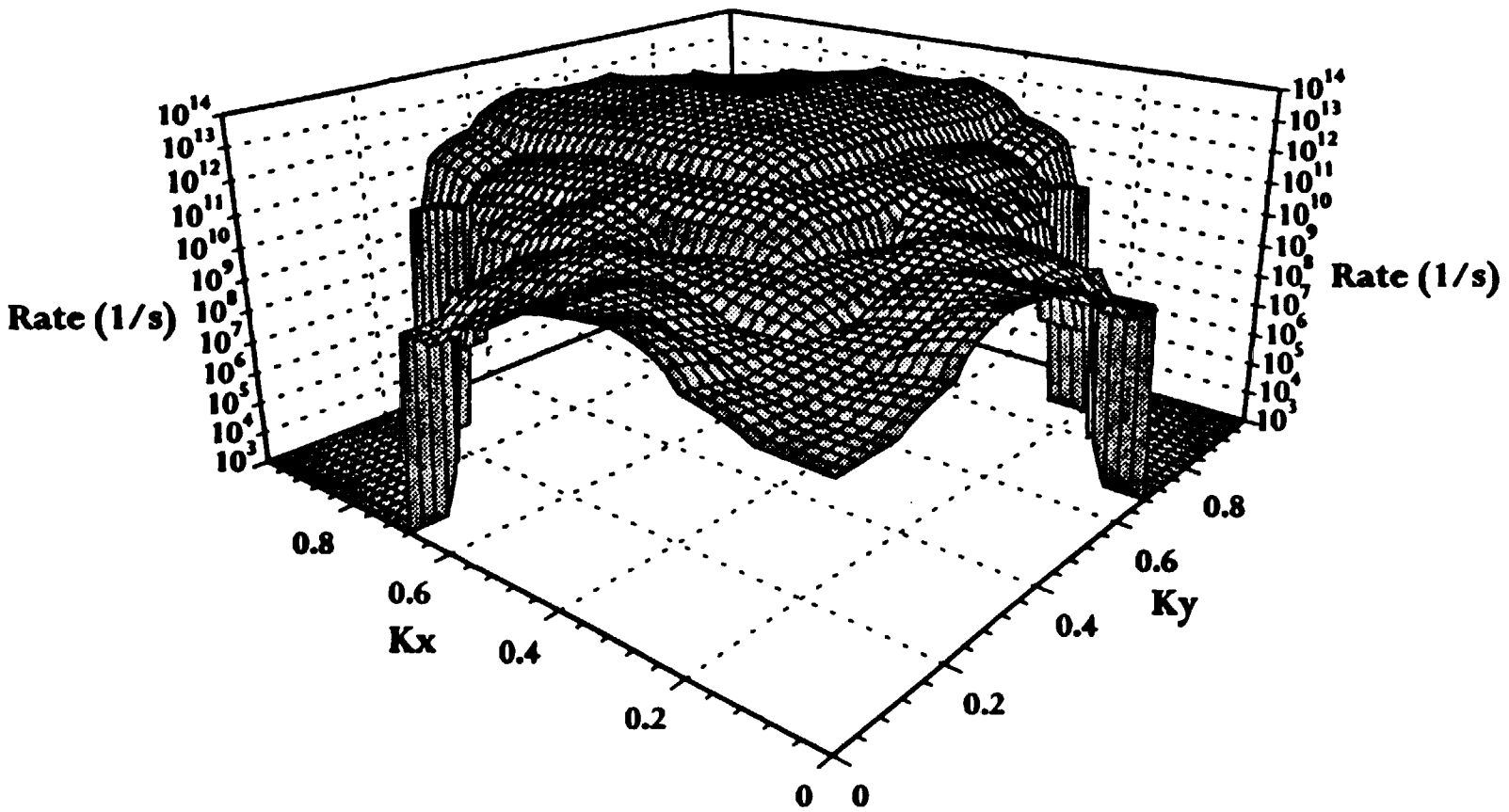


Figure 3.1.3: Impact ionization transition rate as a function of k_x and k_y at fixed k_z=0.0 for the second conduction band of bulk silicon.

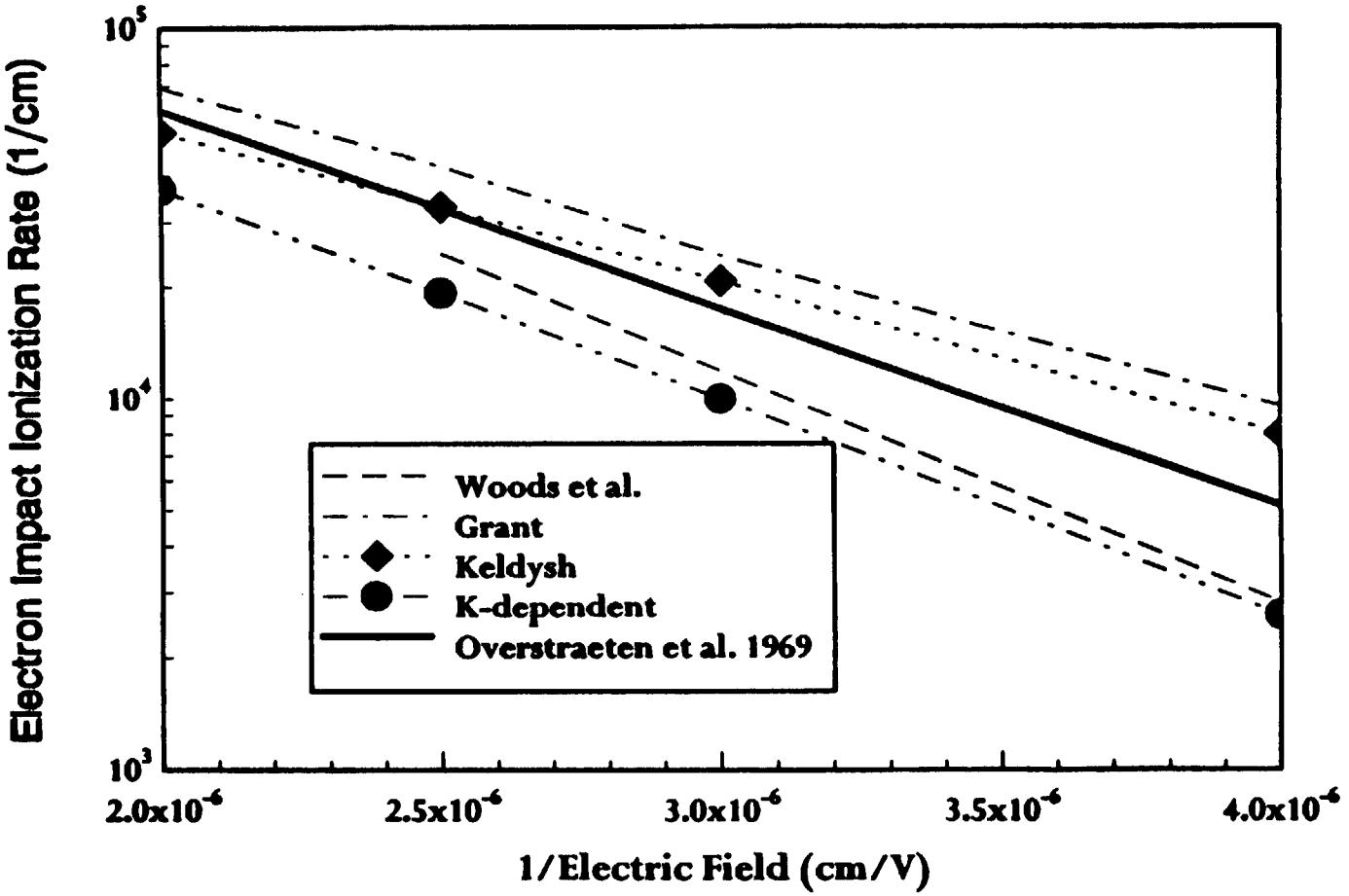


Figure 3.1.4: Experimental and calculated values of the total electron impact ionization rate as a function of inverse applied electric field. Notice that the k-dependent calculations agree well with the experimental measurements of Woods et al.

leading to hole impact ionization. To circumvent this difficulty, we believe it is possible to use a delta-doping technique creating the built-in p-i-n junctions using single layers of dopants. The delta-doped device structure is sketched in Figure 3.1.5. The basic structure is similar to the volume doped device structure in that the basic unit cell is comprised of a built-in p-i-n layer followed by GaAs and AlGaAs layers respectively. The primary difference between the volume doped and delta-doped devices is in the thickness of the doping layers. In the delta-doped design, the doping layers are made from a single charge sheet while in the volume doped devices, several layers of material are doped. Experimental work is progressing towards determining whether use of the delta-doping technique will improve the accuracy of the dopant levels thereby leading to more reliable depletion of each built-in junction.

The performance of different delta-doped device designs have been examined using the Monte Carlo simulator described above [8]. The Monte Carlo calculations indicate that comparable performance between the new delta-doped APD and the volume doped APD can be attained. Subsequently, low-noise operation can be sustained at higher gain levels using the delta-doped APD.

3.1.2 Macroscopic Modeling of HACTs and CTDs

As discussed above, we have developed a macroscopic hydrodynamic model which we have applied to the study of HACTs and CTDs. The hydrodynamic model seeks the self-consistent solution of the continuity, flux and energy flux equations for both the electrons and holes. The variables solved for are the electron and hole carrier concentrations, the

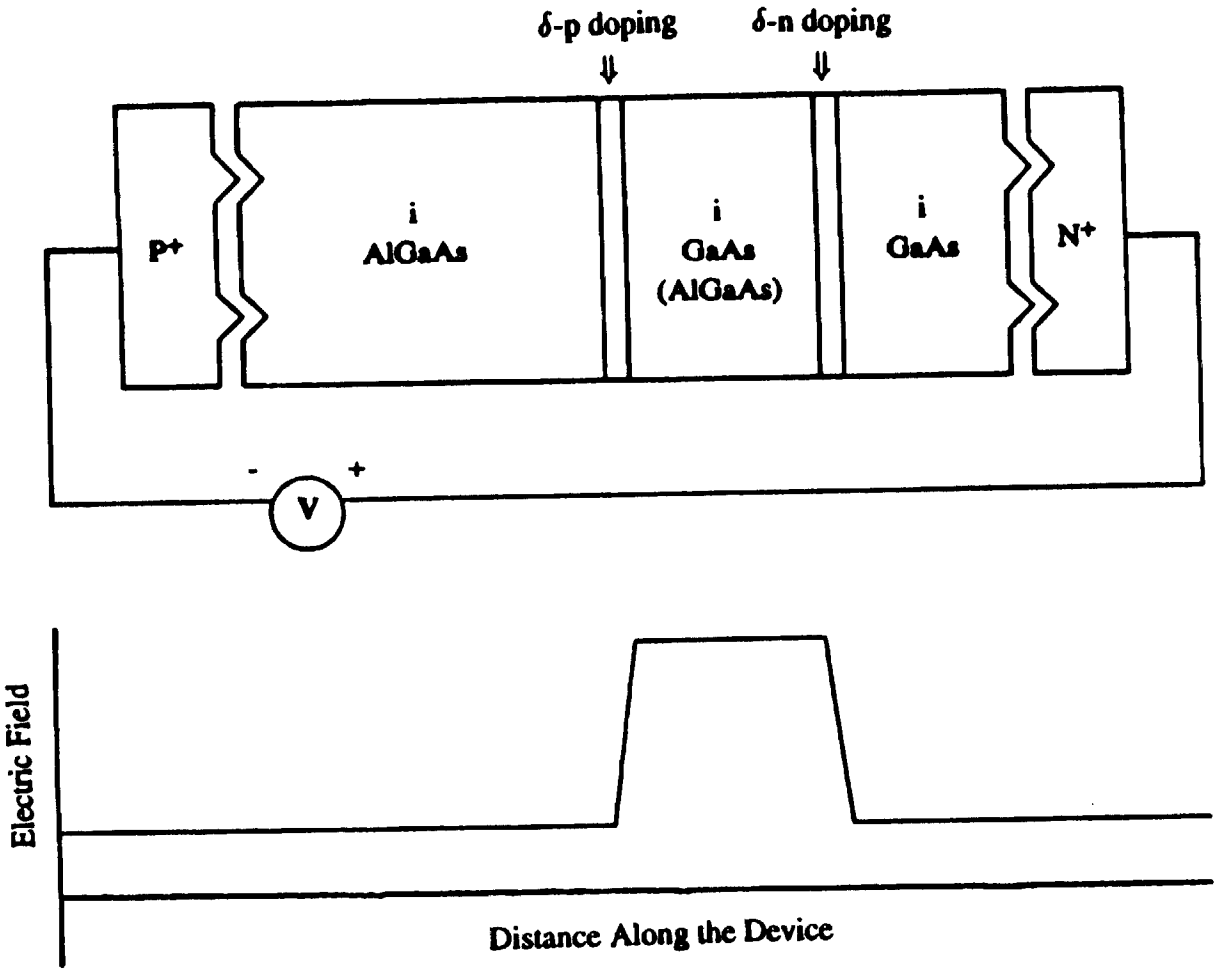


Figure 3.1.5: Schematic drawing of the basic unit cell of a delta-doped APD device along with the corresponding electric field profile.

electrostatic potential, and the electron, hole and lattice temperatures. From knowledge of these variables, macroscopic observables such as the current density, and capacitance which can be compared to experimental results can be readily obtained.

We have studied different HACT designs using the hydrodynamic simulator. The first design examined is a standard structure containing a double GaAs/AlGaAs heterostructure. The primary advantages of this design are that it requires only one doping type and uses two heterojunctions to confine the charge. The disadvantages though are that the design has a high sensitivity to surface state concentration and to the materials preparation. Due to the presence of a large surface state concentration, in order to control the amount of charge within the HACT channel, it is necessary to control the doping levels within the device to extremely tight tolerances. This presents great difficulty in reproducing the device behavior from one sample to the next. A typical device structure is shown in Figure 3.1.6. The corresponding conduction band profile is shown in Figure 3.1.7. Figure 3.1.7 shows the effect on the conduction band profile of the presence of surface states within the top GaAs layer. As can be seen from Figure 3.1.7, the presence of a high concentration of surface states produces a potential barrier between the conduction well of the HACT device and the surface contacts. As a result, charge injection into the conducting channel of the HACT is inhibited. The lowest potential barrier for charge injection is achieved in the absence of surface states. The potential barrier is highly sensitive to the surface state concentration since a change of only one order of magnitude from 10^{12} to 10^{13} leads to a dramatic change in the band bending within the device. Experimental evidence indicates that the surface state concentration is typically around this range.

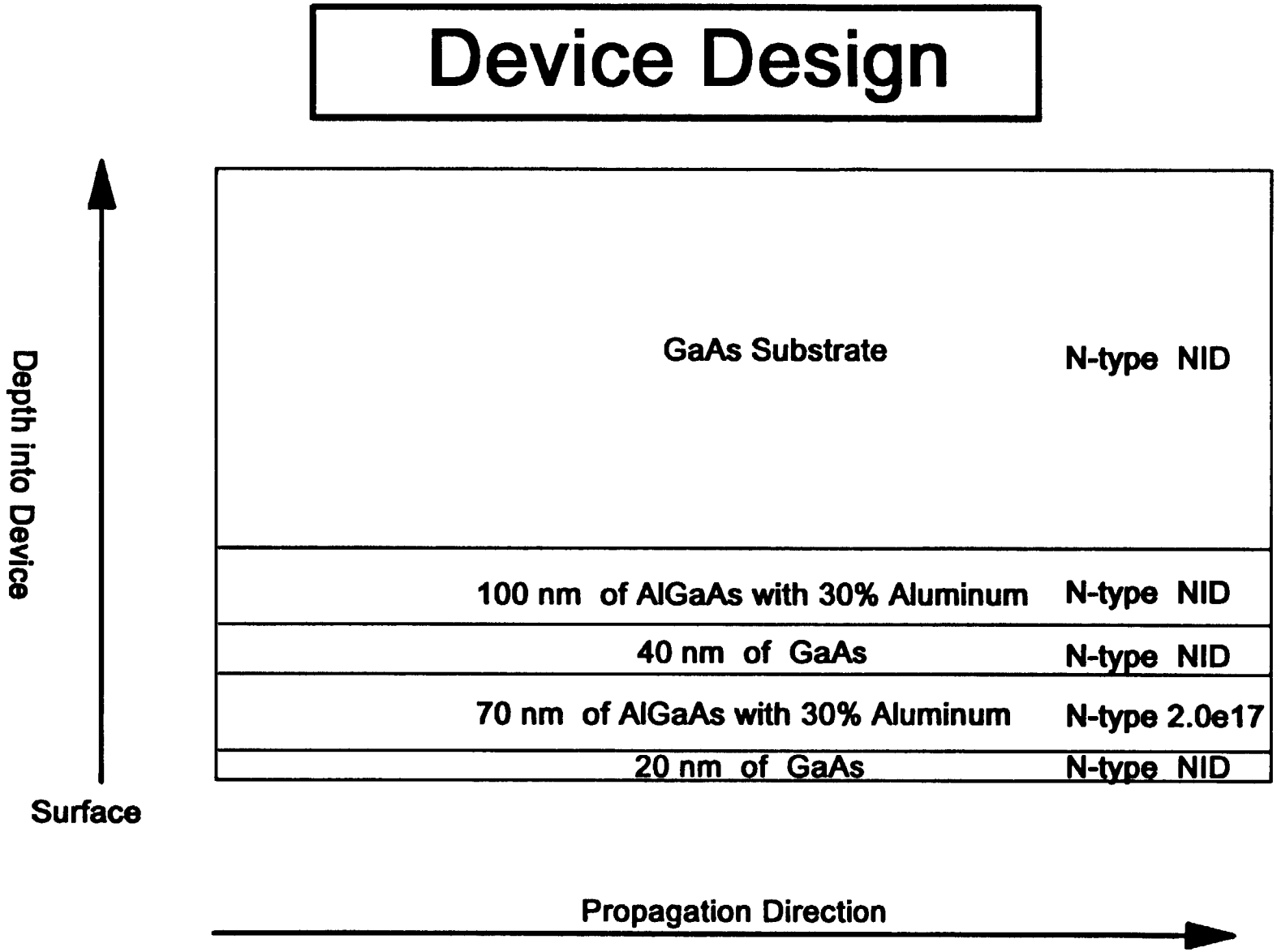


Figure 3.1.6: Sketch of the layer widths and doping concentrations of the first HACT design.

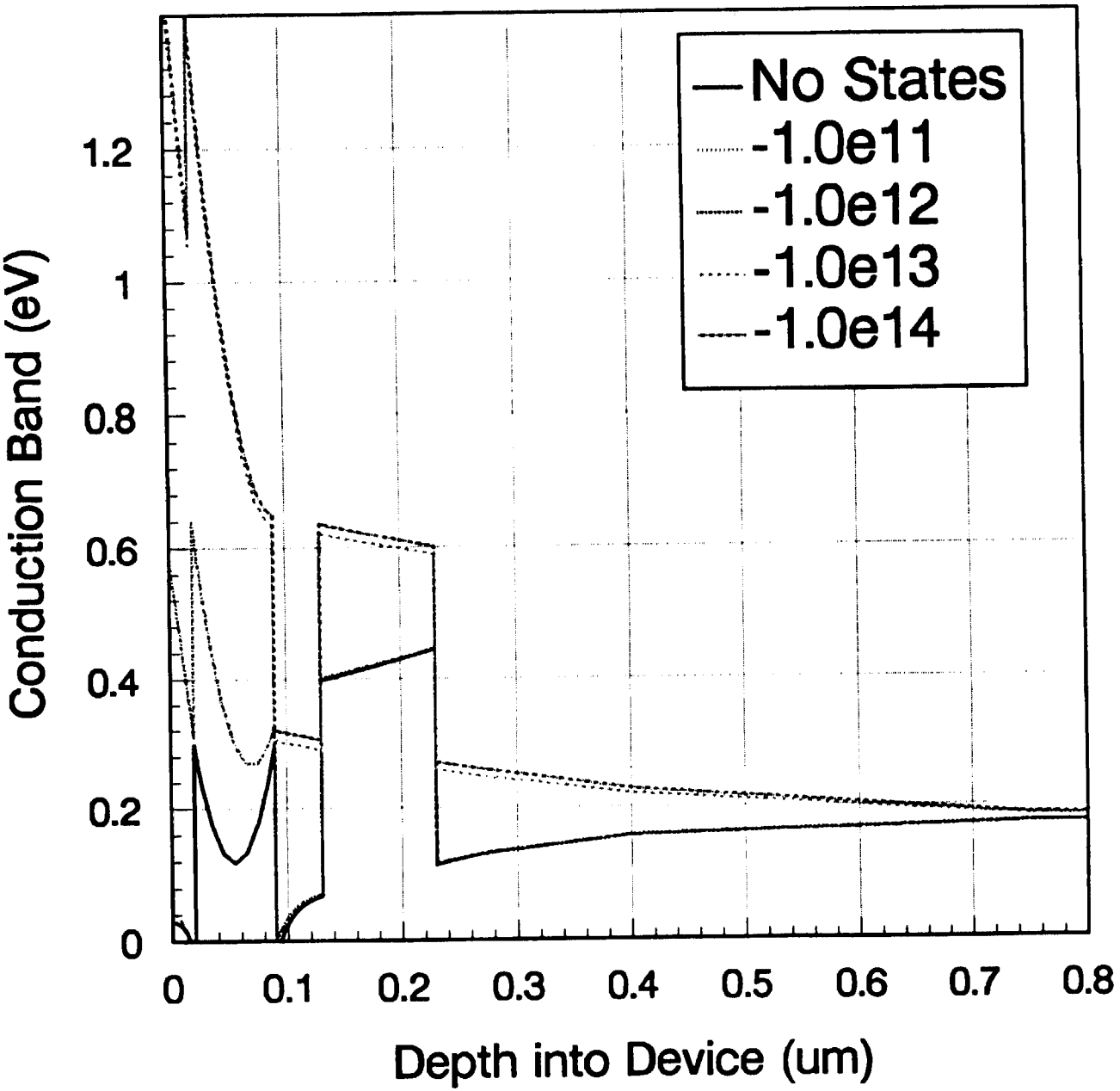


Figure 3.1.7: Conduction band diagram of the first HACT design under different surface

The hydrodynamic simulator also includes the effects of the acoustic potential. A contour plot of the potential as a function of depth into the device is shown in Figure 3.1.8. The second GaAs layer from the top in Figure 3.1.8 is the layer in which the electronic charge propagates. The potential minimum lies within the contour marked 0.221 in the figure. The figure shows good charge confinement in the lateral directions from the acoustic potential and charge confinement in the transverse direction from the heterojunctions. Calculations show that the charge capacity of the potential trough is roughly 10^7 electrons.

We have also examined an alternative ACT structure. In this structure, the surface top layer is made p-type in order to reduce the sensitivity of the device to surface states. The presence of the p-type layer has the additional advantage of simplifying charge injection into the channel. The disadvantages of the new HACT design is that it shows some sensitivity to doping concentration fluctuations and only provides for single heterojunction confinement in the transverse direction. Nevertheless, the sensitivity to doping variations is not high; variations of less than half an order of magnitude in doping can be sustained. The device design is illustrated in Figure 3.1.9. As can be seen from the figure, a thin layer of p-type GaAs is grown on the top of the device over an n-type GaAs layer which serves to confine the charge. The resulting band diagram is shown in Figure 3.1.10. Confinement of the charge carriers is achieved by the band bending from the p-type layer on the top and the action of the heterobarrier on the bottom surface. Inspection of Figure 3.1.10 shows that the device is highly insensitive to the surface state concentration. Fluctuations in the surface state density from zero to 10^{14} have little measurable effect on the band diagram. As a result, this design should prove to be robust to fluctuations in materials preparation.

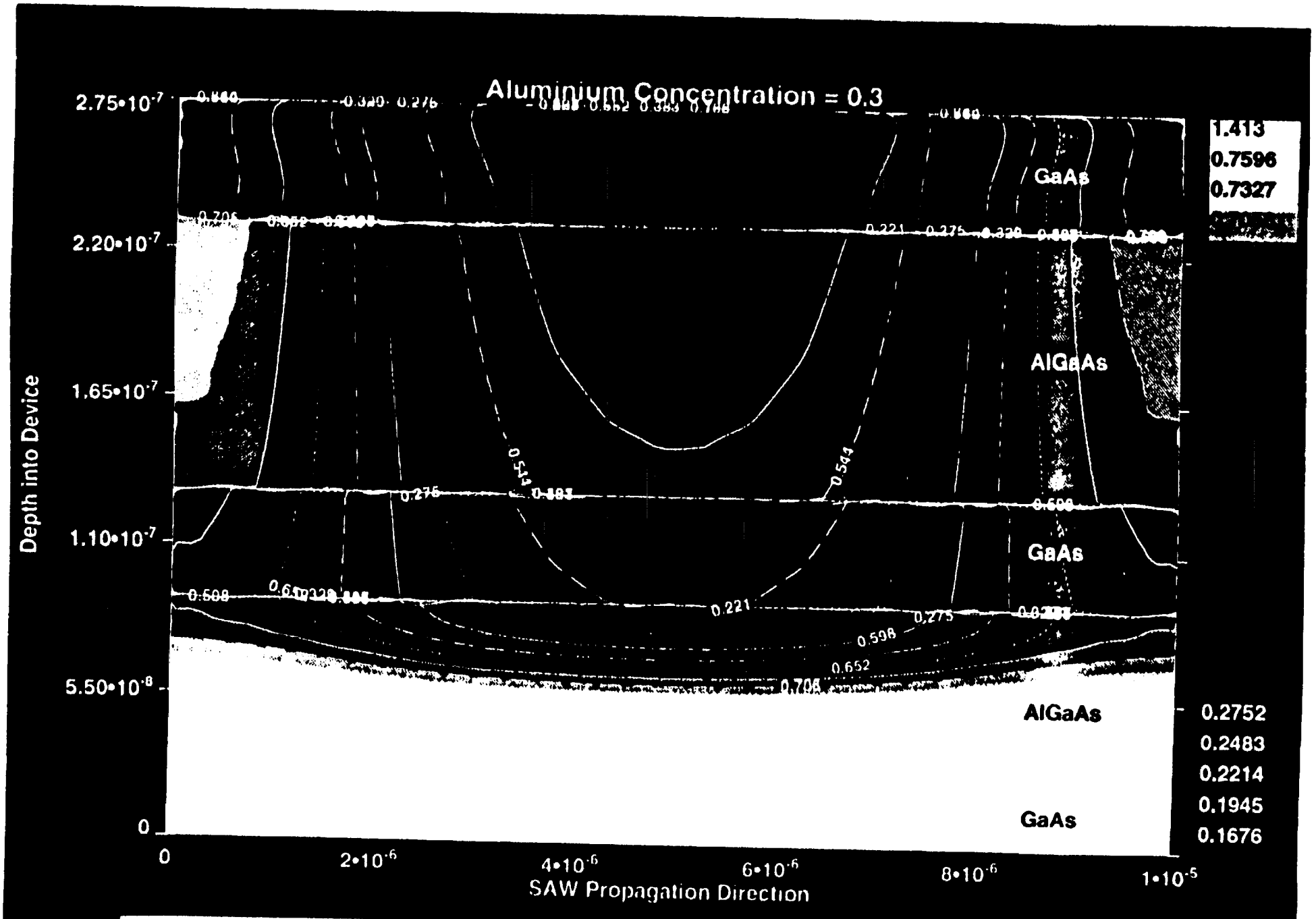


Figure 3.1.8: Equipotential contour plot for the first HACT design. The surface layer lies in the foreground. The SAW wave propagates in the left to right direction in the

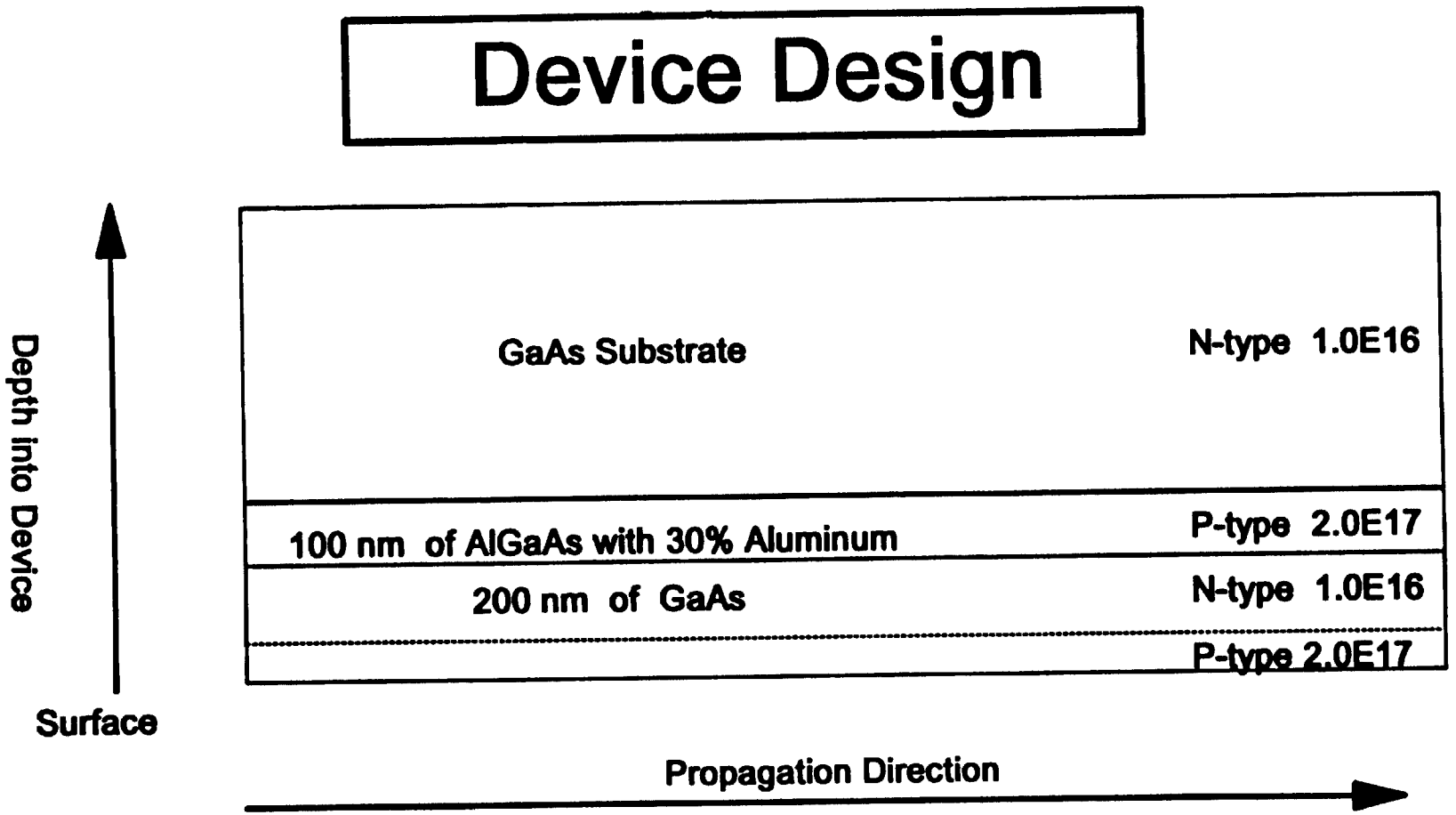


Figure 3.1.9: Sketch of the layer widths and doping concentrations of the second HACT design.

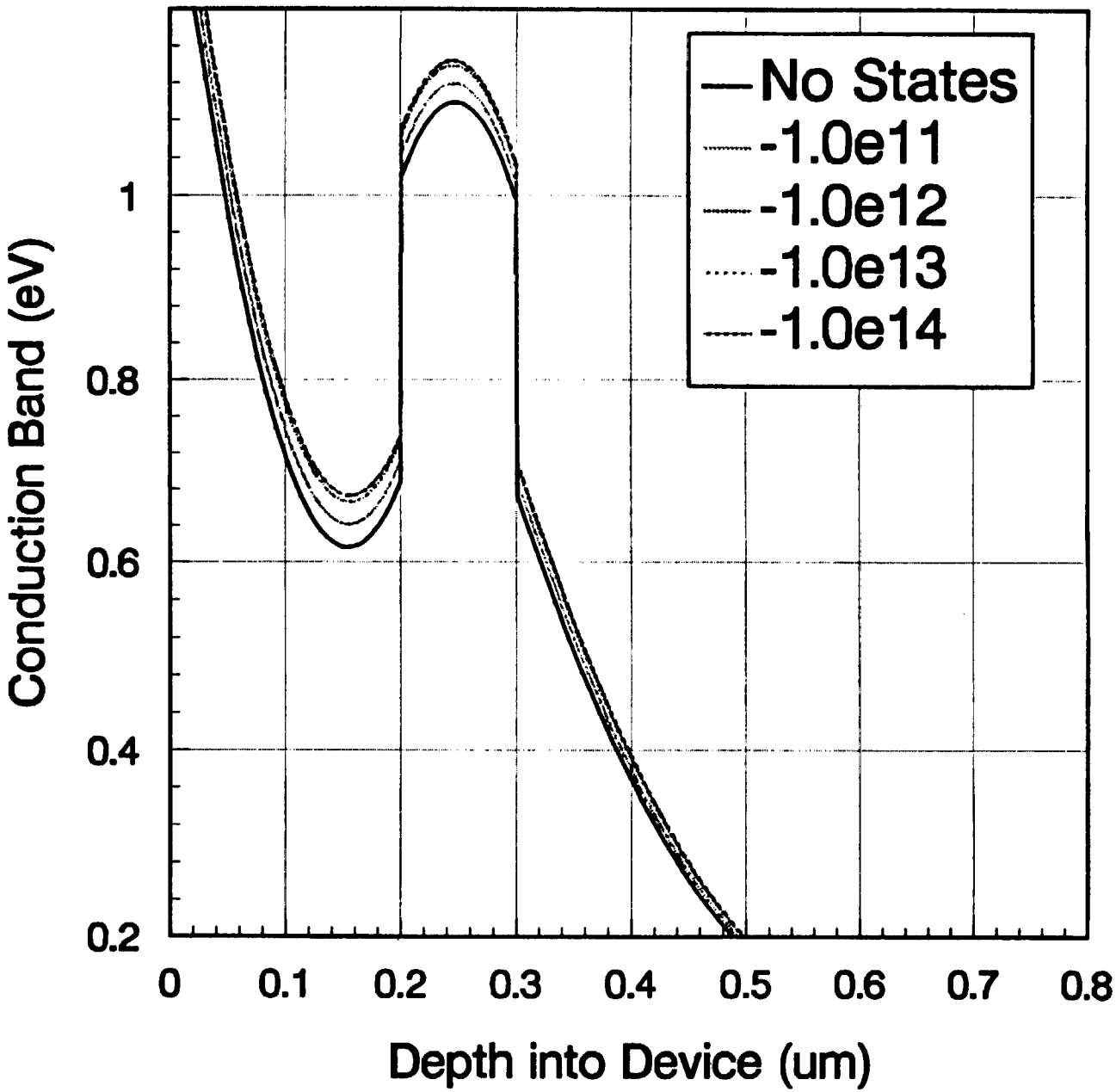


Figure 3.1.10: Conduction band diagram of the second HACT design under different surface state concentrations of no states, 10^{11}, 10^{12}, 10^{13}, and 10^{14}. Notice that the band bending is relatively undisturbed by variations in the surface state concentrations.

A potential contour plot for the new HACT device is shown in Figure 3.1.11. The central ellipse in the figure is the potential minimum within the device. Again, the device shows good lateral confinement due to the acoustic potential. The transverse confinement is due to the heterojunction formed between the GaAs and AlGaAs layers going into the substrate and from the band bending approaching the surface.

The hydrodynamic model has also been applied to the study of the charge transfer device, CTD. A prototype design is sketched in Figure 3.1.12. Owing to the axis of symmetry present along the vertical line, only half of the device is shown in Figure 3.1.12. As in the HACT device, two different CTD designs have been considered to date. The first design utilizes an ion implanted region to form the overflow barrier beneath the overflow contact. The primary advantages of using ion implantation is that no crystalline regrowth is required and the lateral confinement is fixed. Possible disadvantages of this approach are the limitations of the ion implantation process in GaAs. We have had some difficulty in getting reliable ion implants done commercially on our samples. As a result, we have contacted Sandia National Laboratories to assist us in developing a reliable implantation process to ensure uniformity in our devices. A further disadvantage of the ion implanted scheme is that the barrier height is fixed by the dopants; there is no flexibility once the device has been made. The calculated band structure for the ion implanted device is shown in Figure 3.1.13. The storage well lies in the foreground of the diagram between the APD input and HACT readout regions. The overflow barrier lies adjacent to the storage well in the background of the figure.

An alternative CTD design that dispenses with the ion implantation step altogether

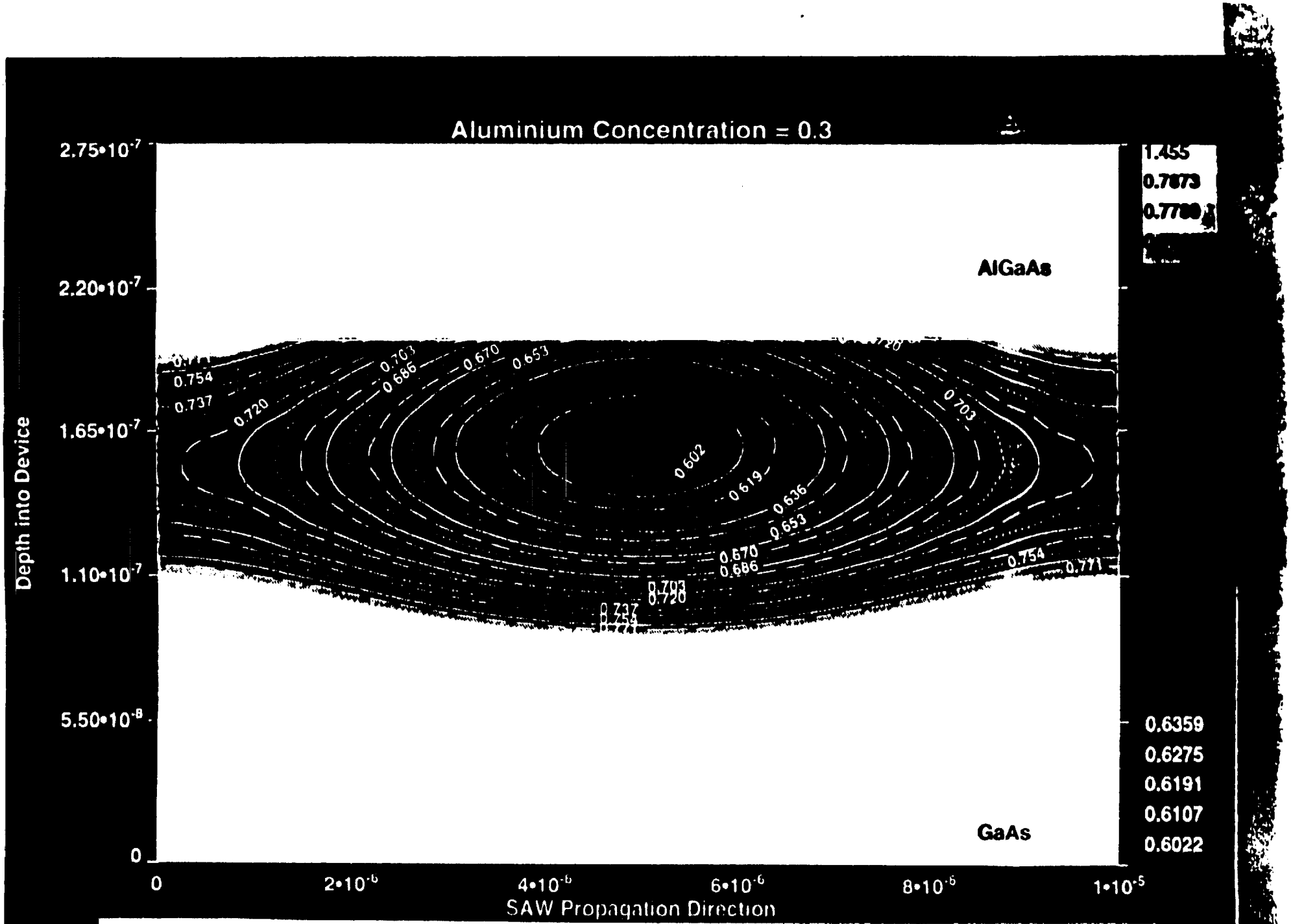


Figure 3.1.11: Equipotential contour plot for the second HACT design. The surface layer lies in the foreground. The potential minimum lies at the center of the centermost ellipse.

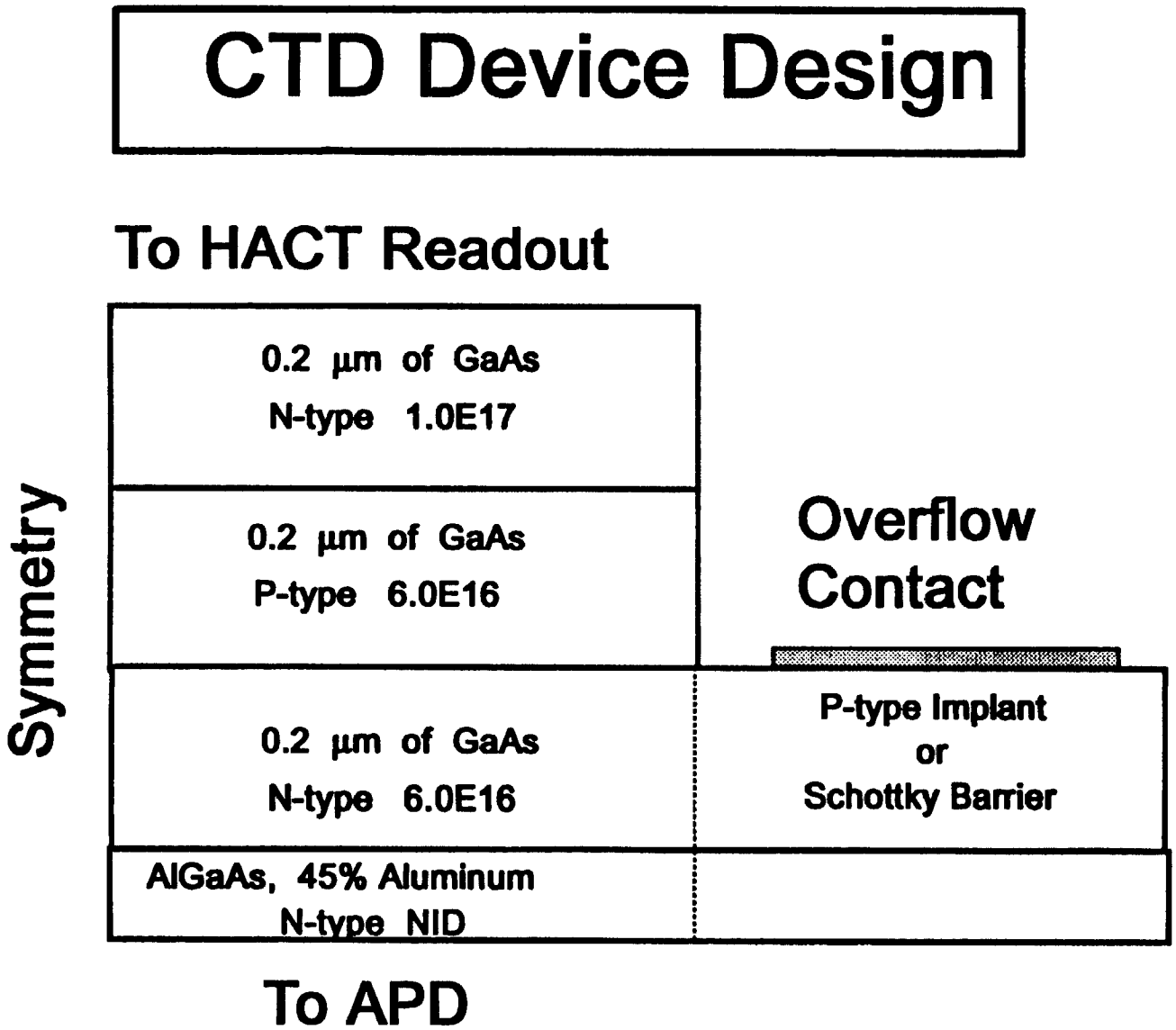


Figure 3.1.12: Schematic drawing of the first CTD design showing layer widths and doping concentrations.

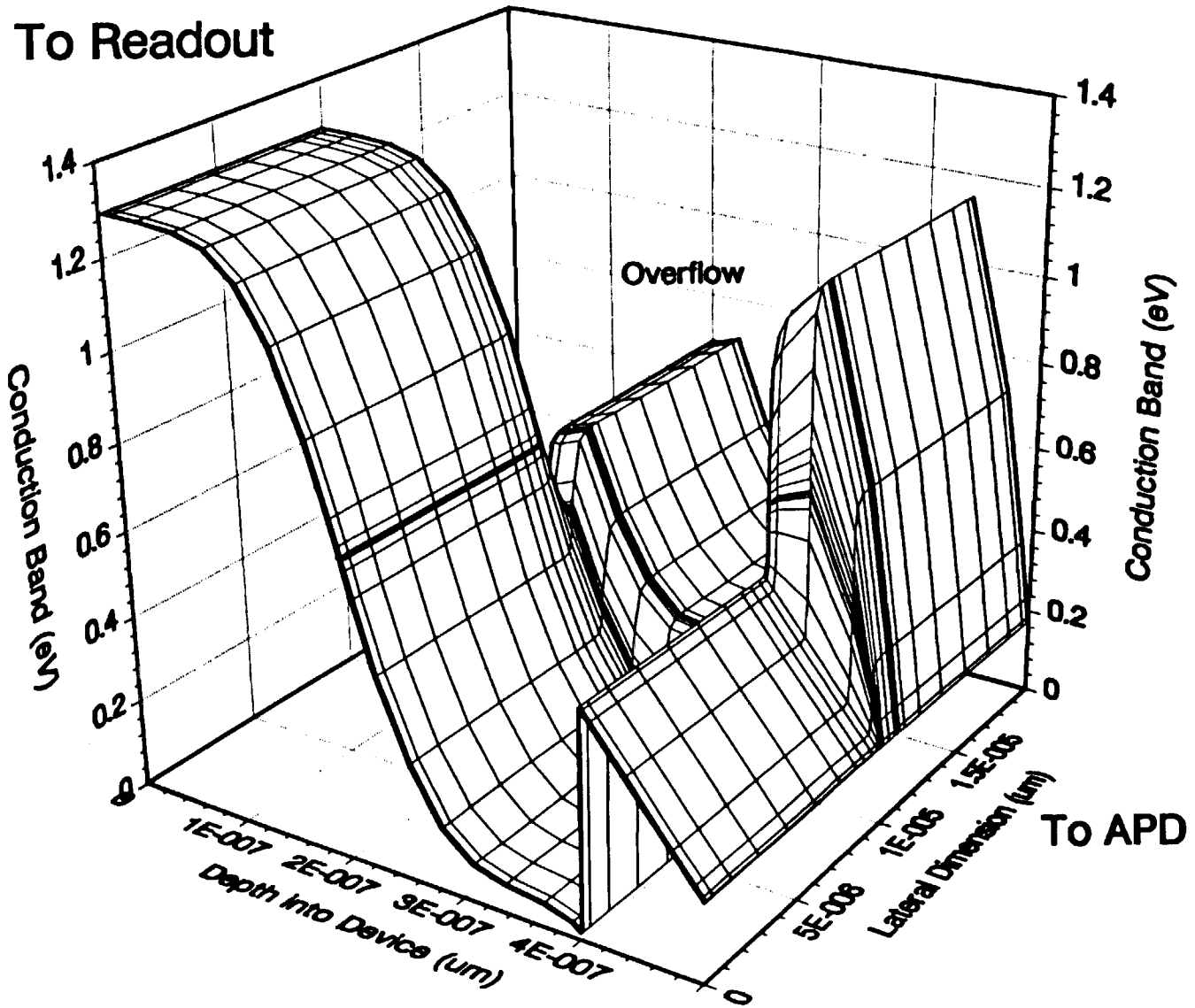


Figure 3.1.13: Conduction band bending diagram of the first CTD design (that with a p-type barrier for the overflow contact). The potential well in the foreground of the diagram is the charge collection well. Charge is read-in from the APD contact, held and then readout into the ACT channel.

utilizes a Schottky barrier contact instead. The primary advantages of this design are that no ion implantation is required and the overflow contact is voltage controllable. However, possible limitations of this design are that it requires a material regrowth using the MBE, and the Schottky barrier may provide a high leakage current leading to a sizeable dark current within the device. The calculated band diagram using the hydrodynamic model is shown in Figure 3.1.14. Again the storage well is the potential minimum lying in the foreground of the figure between the APD input and the HACT readout contacts. The overflow barrier in this case depends upon the applied bias to the Schottky contact. The potential height can be changed by varying the bias depending upon how high a potential barrier is desired. In a later section of this report, we will discuss the charge holding capacity of these devices.

3.1.3 Acoustic Studies for HDTV Imager

An important part of the proposed imager is the SAW which is being used to read out the photogenerated charge. One needs to know the vertical and transverse profiles of the potential propagating with the SAW as it is this potential which transports the photogenerated charge. Great care has been taken to develop the analytical tools which will allow us to optimize the device structure with regard to both its acoustic and electronic aspects and in this section we will discuss the progress made regarding these acoustic design tools.

In Figure 3.1.15 we present the project block diagram with a detailed breakout of the acoustic portion of the Simulation and Design block. For an architecture under consideration the vertical structure is supplied to the program in the form of the thicknesses

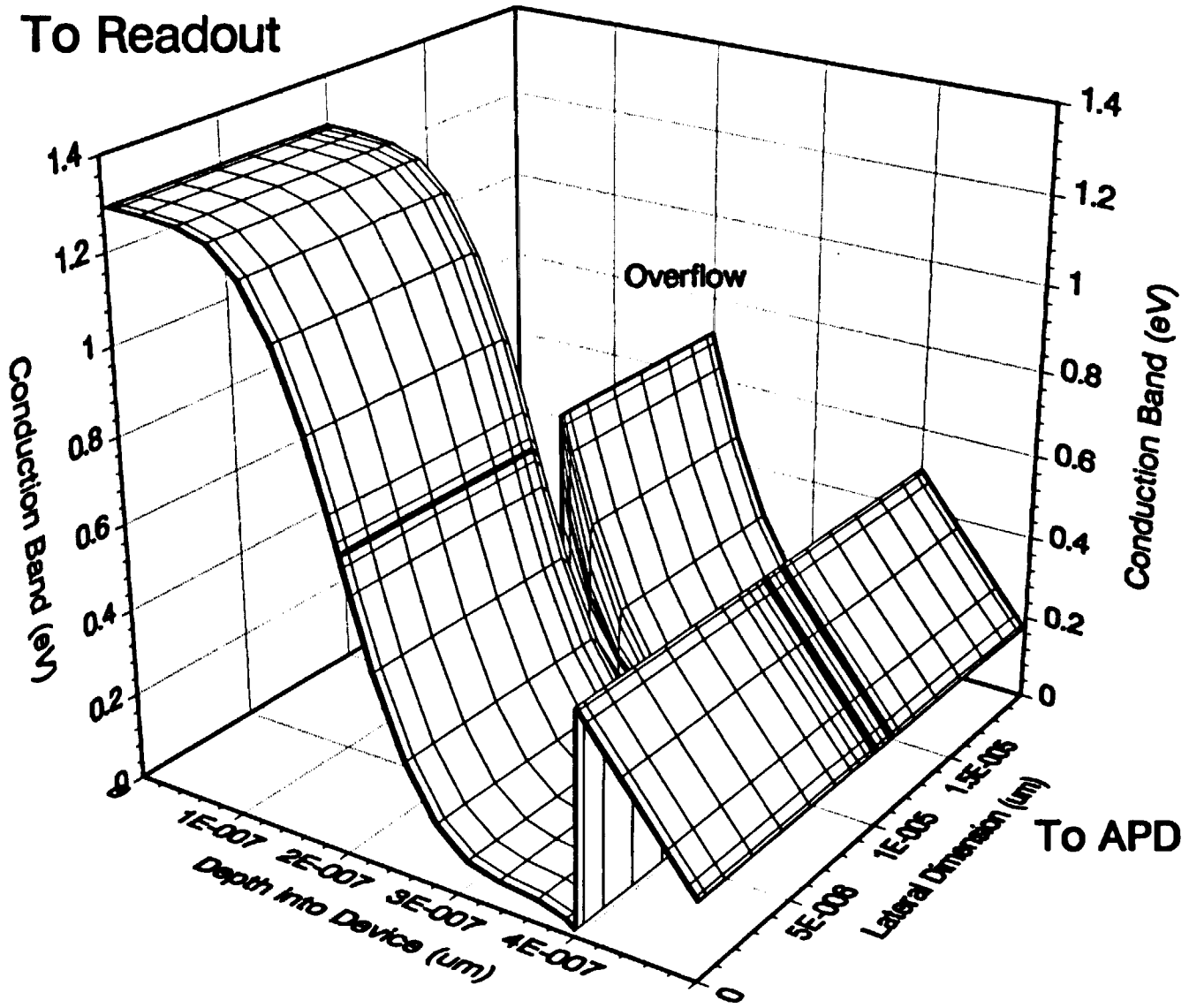
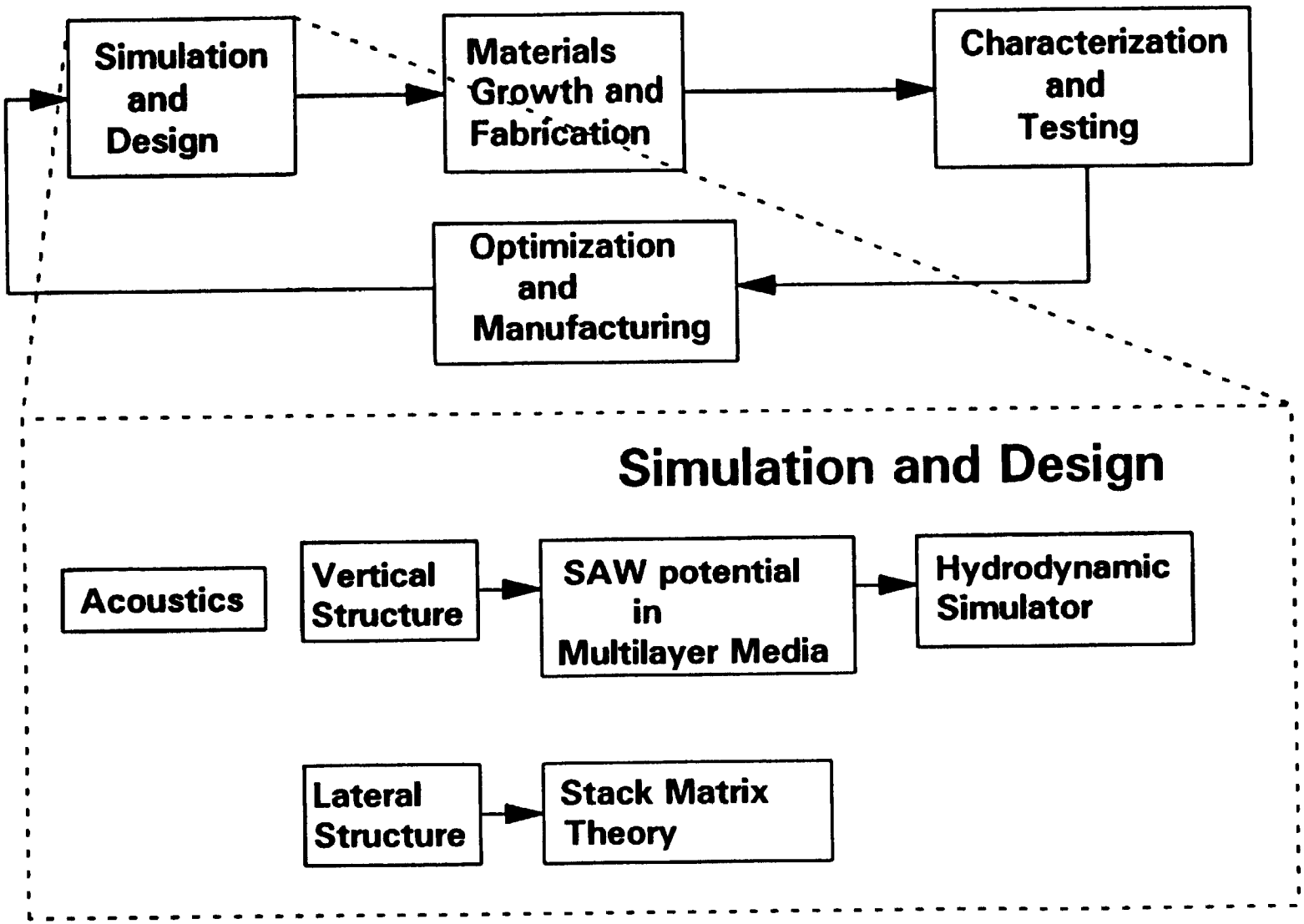


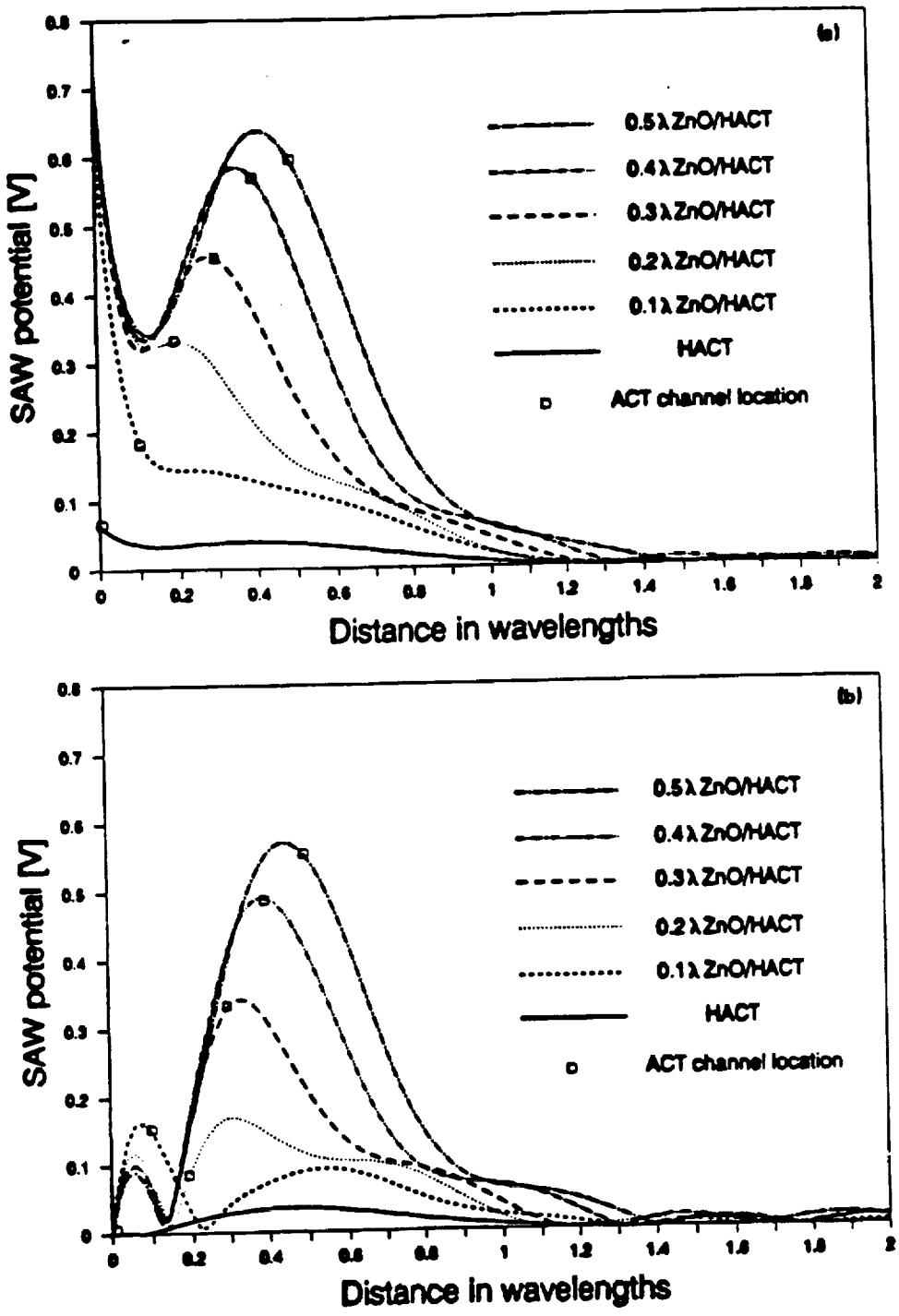
Figure 3.1.14: Conduction band bending diagram of the second CTD design (that with a Schottky barrier for the overflow contact). The potential well in the foreground of the diagram is the charge collection well. Charge is read-in from the APD contact, held and then readout into the ACT channel.



3.1.15 Simulation and Design: Acoustic Design Tools

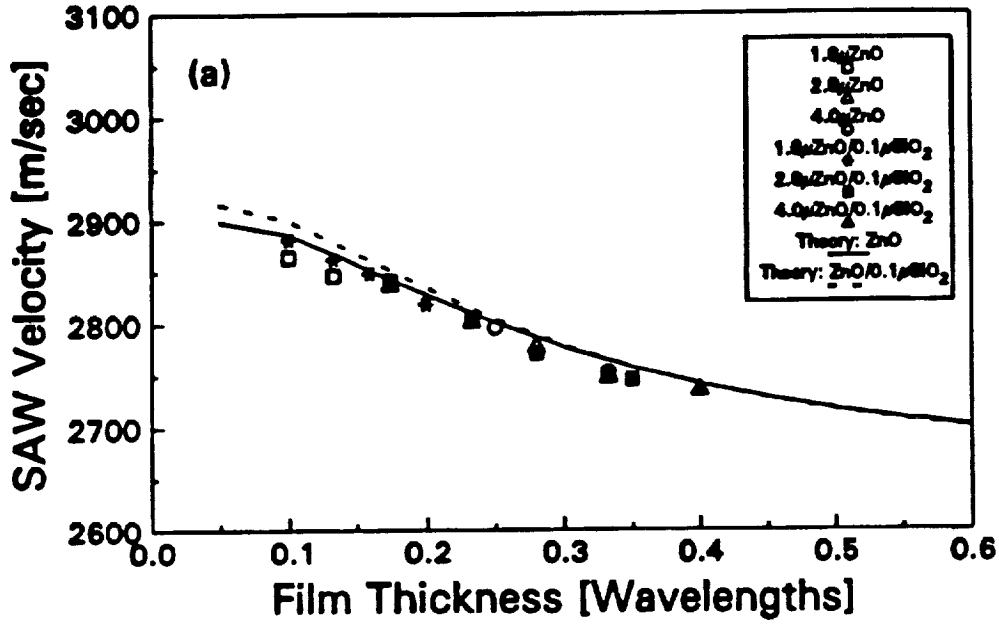
and physical properties of various layers [9]. At the present the physical properties includes the dielectric tensor, piezoelectric tensor, stiffness tensor and mass density. It is the point of future studies to also include any mobile carriers which may be present. For example, one structure under consideration is a thin piezoelectric film, ZnO, overlying the HACT device [10]. The tool has allowed us to establish the appropriate thickness of the ZnO film and all other layers so as to optimize the device structure. An example of the calculated SAW potential for the ZnO overlay structure is shown in Figure 3.1.16. The small square on the figure indicates the location of the charge being transported. As is shown in Figure 3.1.15 the SAW potential computed by the program is then used as an input to the hydrodynamic simulator described in Section 3.1.2. Along with allowing us to predict the SAW potential in a multilayered structure, the program predicts the SAW velocity and piezoelectric coupling coefficient. A comparison between the predicted SAW velocity and our experimental measurements is shown in Figure 3.1.17 [9]. These experiments represent a collaboration between our group at Georgia Tech, Motorola Inc. and the National Research Council of Canada [11], [12].

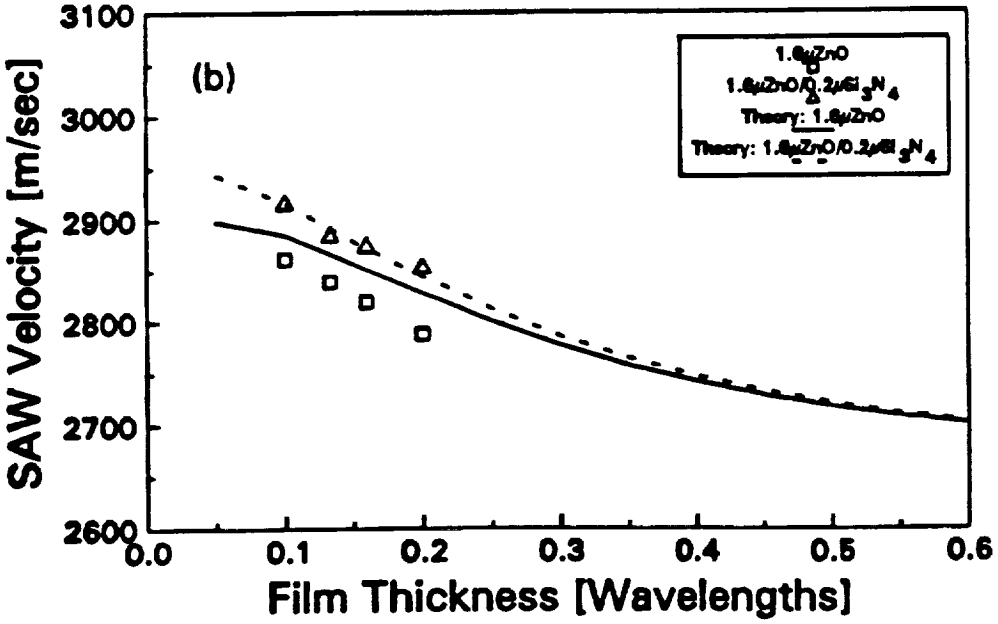
When one considers the architecture of the HDTV imager it is apparent that the electronic structures such as the APDs and the CTDs will form acoustic waveguides. Though we are not to the point in this project where the chip architecture has been solidified it was clear that a tool was needed to allow us to include the waveguiding into the design. As such we developed the Stack Matrix Theory program described in Figure 3.1.15. This program takes as its input the SAW velocities in the various regions that run along the propagation direction and produces waveguide mode profiles and mode frequencies [13].



SAW potential profile vs ZnO film thickness: (a) for open-circuit surface, (b) for short-circuit surface.

3.1.16 SAW potential profile vs ZnO film thickness: (a) for open-circuit surface, (b) for short-circuit surface





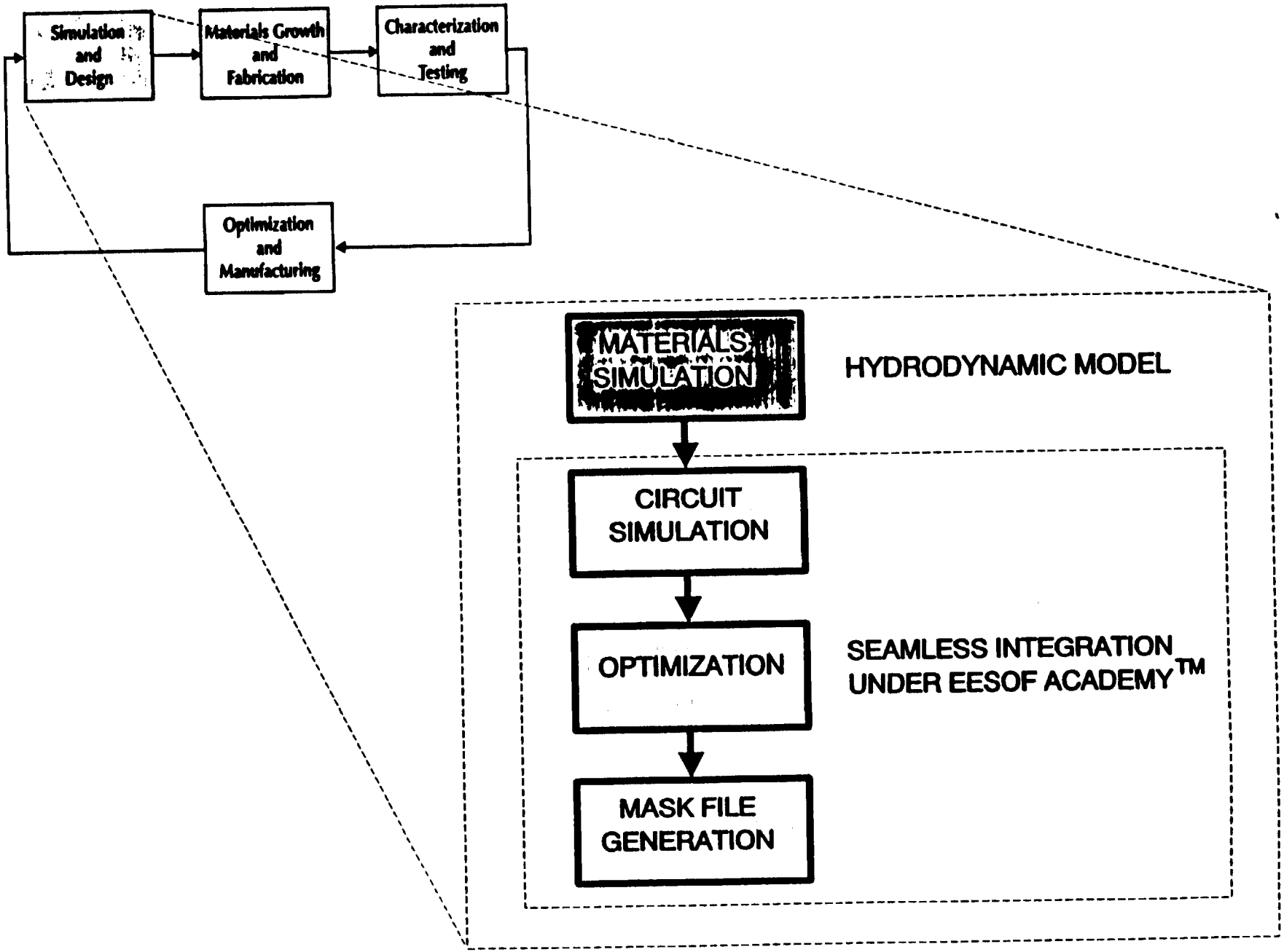
3.1.17 SAW Velocity: A Comparison of Theory and Experiment

With this tool we will be able to optimize the electronic and acoustic performance of the imager array. This tool has been experimentally verified and is being exploited for commercial SAW devices by Bell Northern Research Ltd, RF Monolithics, SAWTEK and Siemens.

3.1.4 Merging Device Simulation and Mask Generation for HACT Devices

In the course of this project we seek in general to develop tools that can enable our industrial partners to commercially exploit our research. As a part of this overall theme, we building macros for a collection of software packages from EESof Corporation which supply us with an environment in which we can simulate the performance of HACT devices *via* physically-based circuit models and will allow us to go directly from this simulation to semiconductor mask layout. At the present time we have only incorporated the HACT devices but in our continuing work on this aspect of the project we will include the APDs and the CTDs so that the entire imager chip can be designed using this seamless integration of simulation and mask layout. This approach is similar to what is used for silicon application-specific integrated circuits (ASICs) where the designer works in a CAD environment thinking only of the circuit functionality and performance even though the result of the work is a computer file which is then used to generate a set of semiconductor masks and ultimately the integrated circuits.

In Figure 3.1.18 we present the project block diagram with a detailed breakout of the portion of the Simulation and Design block related to circuit simulation and mask file generation of the HACT device. From the hydrodynamic model described in section 3.1.2



3.1.18 Simulation and Design: HACT Circuit-Level Model

the parameters for the circuit simulator are derived, thus allowing us to go from the device physics of the architecture to a circuit-level assessment of the performance. Components of this circuit model include charge injection, charge transport and output sensing as shown in Figure 3.1.19. In addition, thermal noise is included in the injection transport and output processes; shot noise is included in the injection process and transfer noise is included in the transport process as well as various noise sources such as thermal noise, shot noise and transfer noise. The various parts of this model have been experimentally verified and in Figure 3.1.20 we present the comparisons for the Insertion Loss and Noise Figure [14], [15].

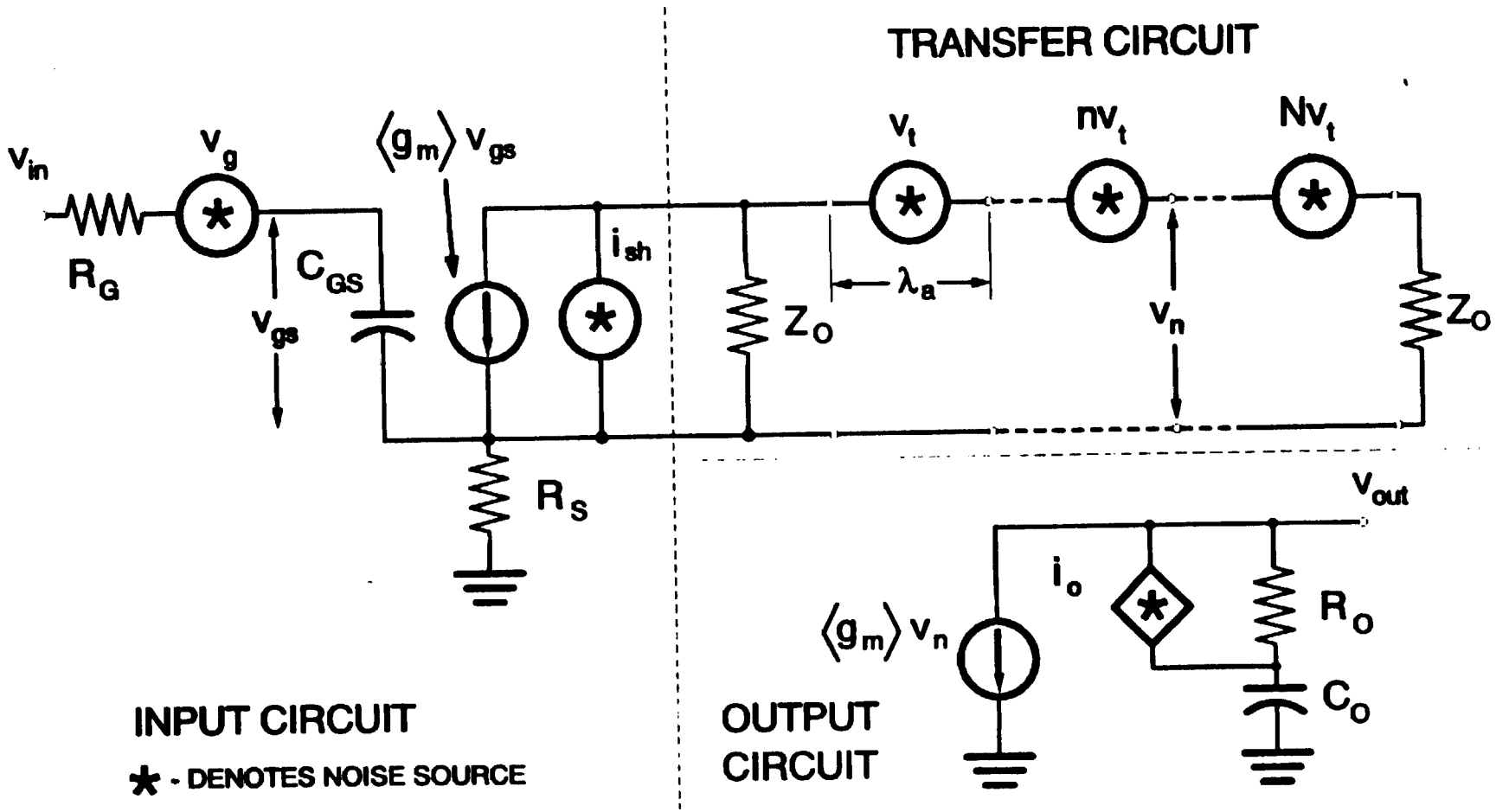
Another advantage of this approach is that it can also be used for yield modelling which leads to our recently-initiated manufacturability studies. In Figure 3.1.21 we present the results of one of these investigations where we have modelled the yield of an HACT transversal filter as a function of the defect density [16].

3.2 Materials Growth and Fabrication

3.2.1 Materials Growth

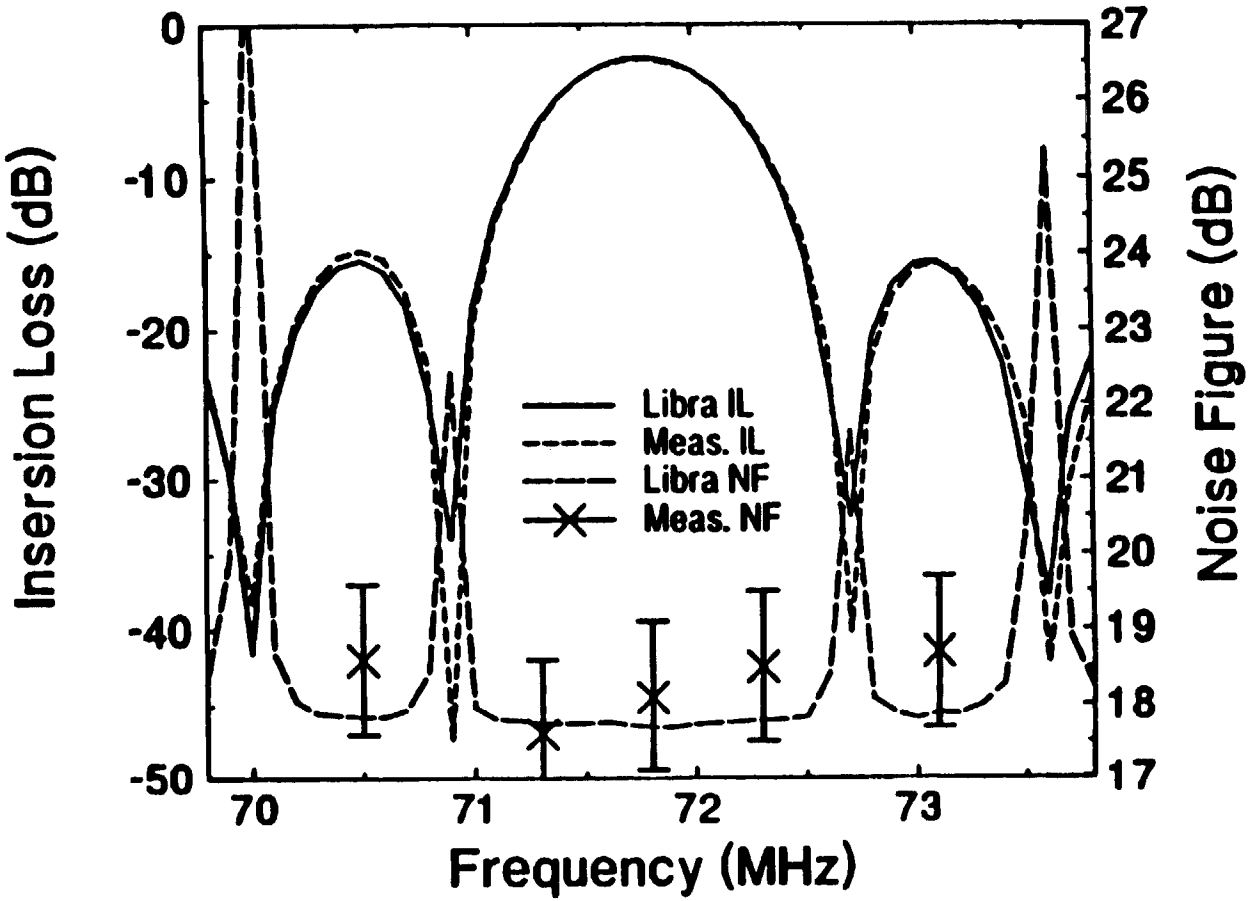
In addition to supplying material for each device in this program, improvements have been continually made to the growth process and system to improve surface and material quality. Among the improvements made to reduce surface defects are the installation of a Ga source with two heater zones and a special dual layer crucible constructed of pyrolytic graphite and pyrolytic boron nitride to minimize Ga spitting, the development of a new substrate holder with indium free mounting (this also reduces the amount of wafer processing required) and the face down mounting substrate holder to minimize electrostatically attracted

HACT EQUIVALENT CIRCUIT MODEL



3.1.19 HACT Equivalent Circuit Model

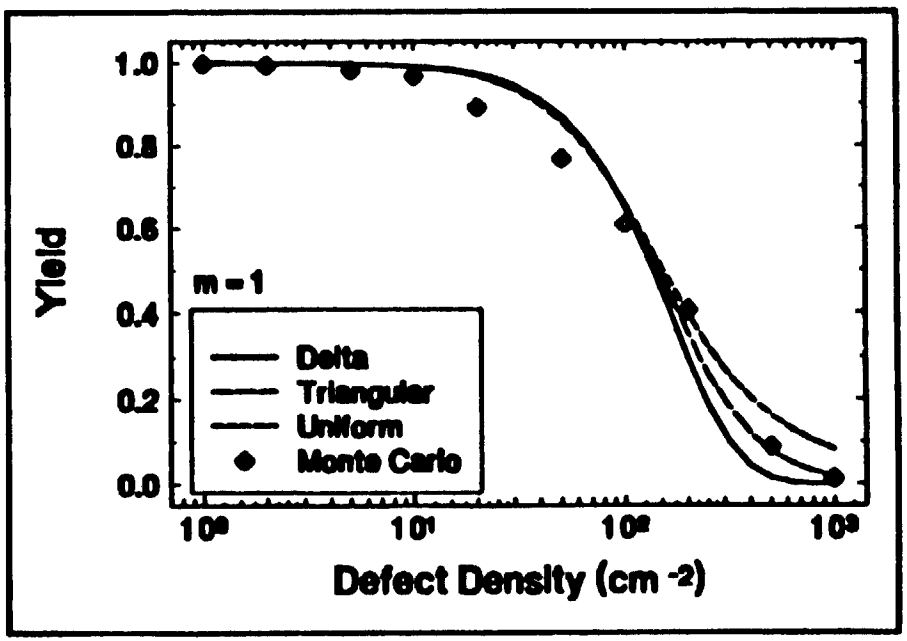
LIBRA™ MODEL FOR 160 TAP HACT DEVICE



3.1.20 HACT Model Results: Insertion Loss and Noise Figure

YIELD SIMULATIONS USING LIBRA™

- 500 TRIAL MONTE CARLO FREQUENCY RESPONSE SIMULATION OVER RANGE OF DEFECT DENSITIES



3.1.21 HACT Yield Simulation Results.

particulates. Another addition to the system is a class 10 laminar flow hood/glove box combination attached to the MBE load lock. Other system improvements include a infrared pyrometer to allow accurate substrate temperature measurement at 0.97 μm and longer wavelengths and the implementation of a calculation of thickness uniformity for the given geometry of our MBE system, sources and shapes of crucibles.

These modifications have led to an improvement in material quality. For example, a total surface defect density of 47 cm^{-2} over a 2" diameter wafer has been achieved with an oval defect density of less than 20 cm^{-2}. A high degree of thickness uniformity has been demonstrated by the evaluation of quantum well photoluminescence (PL) obtained across a wafer and the flux stability and vertical uniformity has been established by growing 10 periods of a set of quantum wells and measuring identical PL from all wells. In similar structures, an interface abruptness of less than 1 monolayer has been attained as determined by further analysis of the PL emission. Also, accurate AlGaAs alloy composition control has been verified from secondary ion mass spectrometry (SIMS) evaluation of a layered structure.

As a further characterization of the growth system, several Si-doped AlGaAs and GaAs layer were grown and their electrical properties evaluated. These results show an exponential dependence of the AlGaAs carrier concentration on the inverse Si source temperature down to doping as low as $8x10^{15}$ cm^{-3}. This indicates that there is the low level of defects in the AlGaAs required for HACT device operation.

3.2.2 Charge Transfer and Overflow Device

Significant progress has been made in the fabrication of CTDs for the acoustic charge

transport device. The goal of this work was two fold: (1) to determine the optimum device structure which satisfied the requirements for the imager and (2) to develop a fully documented, robust fabrication process which gives high yields, is easily integrated with APD and ACT fabrication, and which can be transferred to industry for imager manufacturing. Current progress on the CTD is highlighted by the first observation of charge transfer in the most recently fabricated devices from process run CTD-5. At this time five process runs have been completed, with another run in progress. The process flow for CTD fabrication is described below.

CTD fabrication begins with the generation, through device simulation, of a material structure based upon the desired device properties or experiment goals. The characteristics of the material structure are studied using the hydrodynamic simulator described earlier. For example, the goal of the current process run, CTD-6, was to isolate the optimum material structure for vertical charge confinement. The range of material structures to be tested in CTD-6 were arrived at by the use of the simulator. For example, Figure 3.2.1 shows the conduction band structures considered, including vertical confinement using a p-type volume doped, p-type delta-doped, and an AlGaAs layer.

After a decision was made on the necessary material structures, these structures were grown in-house by MBE. To date 18 two inch wafers have been grown for CTD fabrication. All these samples have been grown on highly doped GaAs wafers which were delivered with an 'EPI-Ready' surface finish, to minimize particulate contamination. After growth, surface defect densities are optically measured for each wafer, with best values of 176 cm^{-2}. These surface defect densities compare very favorably with values quoted by other researchers in

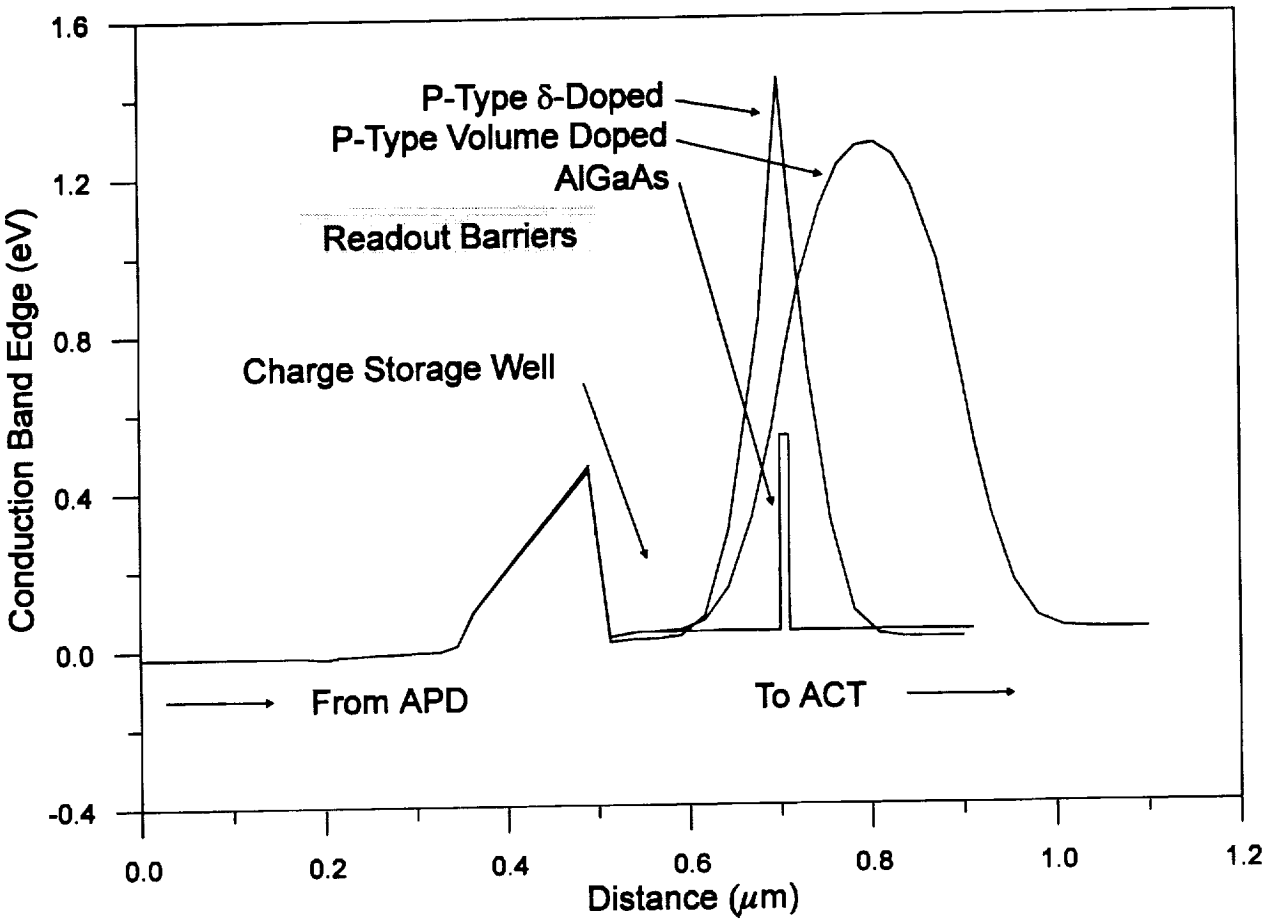


Figure 3.2.1. Equilibrium conduction band diagram for CTD readout barriers, as calculated by the hydrodynamic simulator.

the field. From this point the wafers were submitted for device fabrication.

The CTD device requires a 7 mask set process, where the mask set was designed in-house. The last two process runs used a revised mask design, which incorporates a number of enhancements. These include individual numbering of devices within a die to facilitate testing, an implant protect mask to prevent junction shorting, p-ohmic before n-ohmic processing for optimized rapid thermal annealing, gold plating of all bonding pads for improved assembly, and the addition of test devices across the wafers for validation of material quality and processing.

An important feature of the new mask set is the ability to make '2-terminal' devices in addition to the standard '3-terminal' devices. In the 2-terminal device, the charge overflow mechanism is not implemented, as opposed to the 3-terminal device which utilizes a p-type ion implantation into the n-type barrier layer. However, lateral isolation of the charge storage well is still required, and is achieved using mesa etching. There are several reasons for using the 2-terminal devices at this time. First, the primary function of the CTD, that is an easily filled and emptied storage well for the signal charge from the APD, can be tested without the presence of the overflow mechanism. Second, by neglecting the overflow mechanism for now, the long lead times and problems associated with ion implantation and dopant activation are eliminated. Therefore, CTD devices can be fabricated with greater speed so as to quickly test and optimize different material structures for vertical confinement. Once the CTD material structure has been defined in the 2-terminal devices, the lateral isolation and overflow mechanism can be studied.

The last CTD process run, CTD-5, was on the baseline material structure, which

utilized a p-type volume doped top barrier. The devices were mesa-isolated with diameters of 8, 10, 20, and 40μm, and contact to the readout ohmic was made via an airbridge structure, as in the previous runs. DC current-voltage (I-V) measurements have been performed before packaging on selected devices across the wafer for yield analysis, in keeping with the goals of the project. In these tests, data was taken from the 4 devices of the middle set of each die, for a total of 65 devices. Examples of the different device characteristics are shown in Figure 3.2.2. Good devices showed the electrical characteristics of back to back p-n junctions, as would be expected for this material structure. However, bad devices showed the electrical characteristics of a leaky p-n junction. Through the use of the before-mentioned test structures and the analysis of the ohmic contact rapid thermal annealing data, the device failure was traced to punchthrough of the n-ohmic metallization through the readout layer into the p-type volume doped top barrier, thus shorting out the charge confinement mechanism. This problem will be addressed in future runs through the use of Pd/Ge metallization, which is based on a solid phase reaction rather than alloying, thus yielding less penetration into the readout layer. Despite this problem, proper device operation was observed on 82.8% of the tested devices, demonstrating the maturity of the current fabrication process.

The variation in operating parameters of CTDs across the wafer was also accessed, since device uniformity is critical to successful imager operation. Figure 3.2.3 shows two histograms for the negative and positive readout breakdown voltages for the good devices tested from CTD-5. The average breakdown voltages for positive and negative readout biases were 5.17V and 10.95V, respectively, with standard deviations of 16.7% and 13.5%,

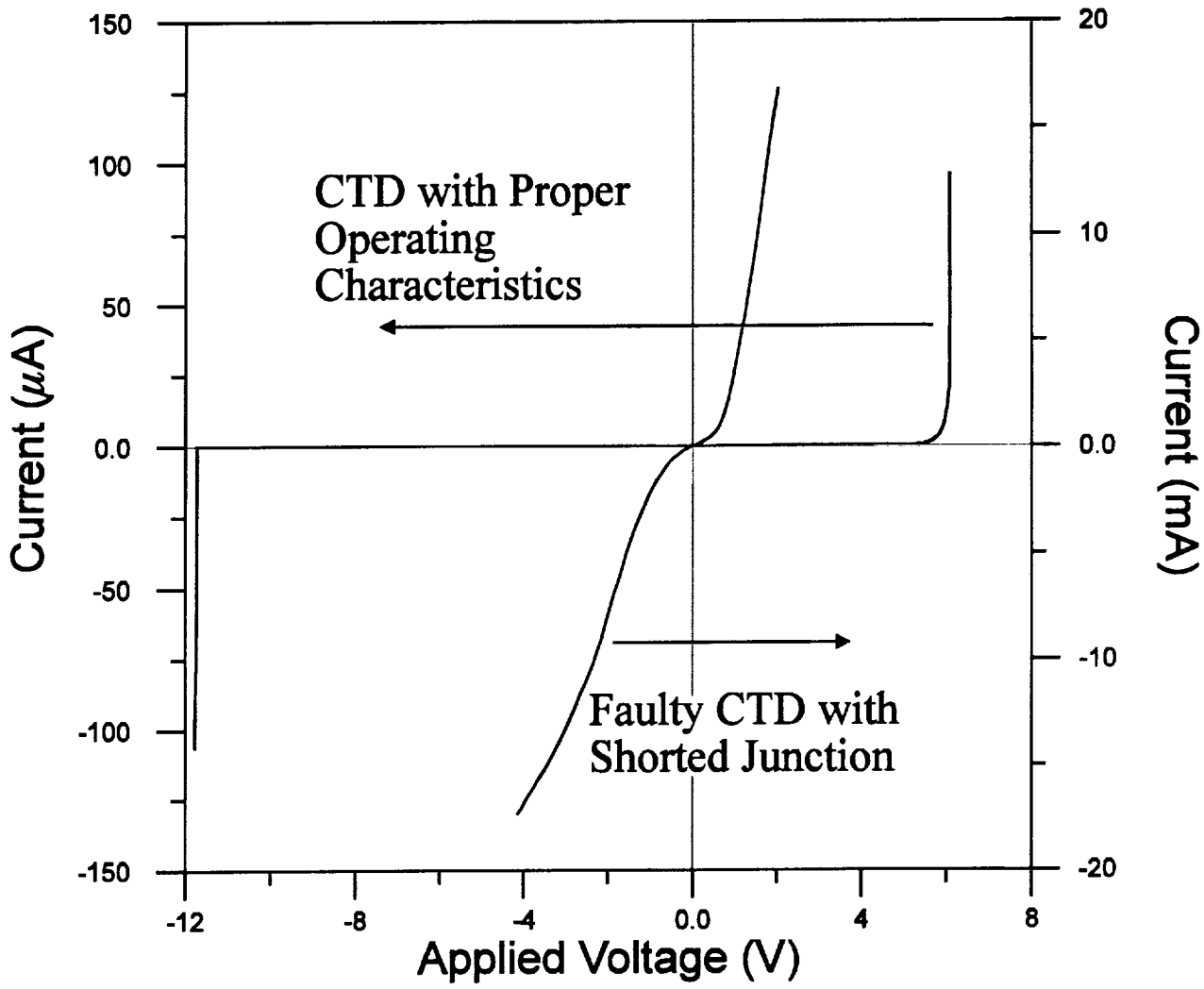


Figure 3.2.2. Current-voltage characteristics measured for 2-terminal CTDs from process run CTD-5.

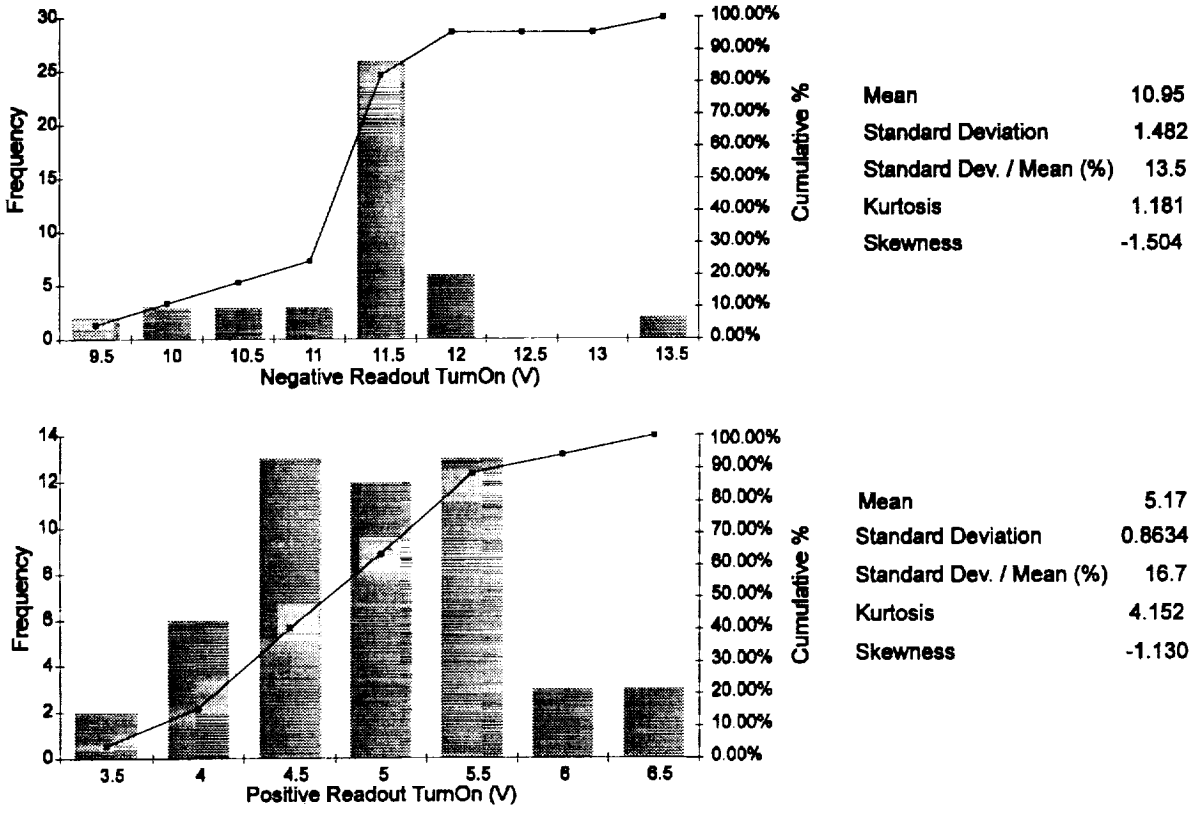


Figure 3.2.3. Histogram and associated statistics for the variation in readout breakdown voltages for positive and negative biases. Data is from process run CTD-5.

respectively. These variations in operating parameters are acceptable at this point in CTD development, and will improve with further process development. For voltages away from the breakdown regions, all tested devices displayed low leakage currents of less than 100nA, thus demonstrating a robust CTD process coupled with low defect density material.

3.2.3 Heterojunction Acoustic Charge Transport Device

During this reporting period excellent progress was made on the fabrication of the heterojunction acoustic charge transport (HACT) device. Specifically, the difficulties with the ohmic contacts and the Schottky diodes have been overcome and as a result, working devices were fabricated. A prefabrication method of measuring sheet resistance was used and a new packaging scheme was instituted to aid in testing. Statistical process control was also implemented to aid in modeling and characterization.

Working Devices

During the past months, working HACT devices were fabricated at GTRI. These devices exhibited good DC characteristics which closely correlated with the theoretical parameters and produced charge transfer efficiencies of 0.99. These wafers were doped at $2x10^{17}$ cm^{-3} with sheet resistances measured by the M-gauge to be approximately 5800 ohms/square. Testing showed that the optimum sheet resistance should be near 5000 ohms/square and material is currently being grown to match this specification.

Ohmic Contacts

Various methods for fabricating ohmic contacts have been used in the course of the process development. The process that is currently producing the best results consists of a

pre-evaporation clean in diluted ammonium hydroxide (1:10 with DI water) to remove any oxides on the substrate after the pattern has been developed. Hot filament evaporation was used to deposit 800Å of gold-germanium (88/12), 100Å nickel and 1000Å gold. The unwanted metal was removed with a liftoff process. The contacts were then alloyed in a rapid thermal processor at 365°C for 30 seconds. Recent devices exhibited contact resistances of 0.47 ohms-mm; by far the best seen to date on material doped at $2x10^{17}$ cm^{-3}. In addition, the resistance from the input contact to output contact was typically 39 ohms.

The quality of the contacts was further verified by the use of SEM and X-ray analysis. These tests verified that the alloy process was diffusing the contact metal through the cap layer and into the channel. Further improvement of the contacts is a goal for the upcoming quarter.

Schottky Diodes

The previous problems with the Schottky diode characteristics were also eliminated with the following process: After the Schottky layer was developed it underwent the same ammonium hydroxide clean as used for the ohmic contacts. The metallization consists of 500Å titanium and 3000Å gold. The platinum was removed from the process due to the power needed to evaporate the metal. The high power produced high temperatures which, in turn made the liftoff very difficult and decreased yield. The titanium worked well as a barrier and also evaporated at a much lower power.

The excess metal was then removed with a liftoff process and the diodes tested. The input Schottkys of the devices showed reverse leakage current at -2 volts of 374 nA with ideality factors of 1.39. During the upcoming quarter the ideality factors and the reverse

leakage current will be optimized.

Sheet Resistance Measurements

A new, non-contact method for measuring sheet resistance was investigated with promising results. The M-gauge by Tenor uses a non-contact, eddy current technique to measure the sheet resistance of unprocessed 2" wafers. With this device, material can be evaluated before processing to eliminate wafers with unacceptable sheet resistance. This prevents wasting time on processing a wafer that has little chance of producing a good device. Currently, a correlation between the M-gauge measurements and the device performance are being investigated.

New Packaging

A new packaging scheme and test setup was designed to improve the quality of the measurements and to decrease testing time. The new package has less die area in a 16 pin dual inline package. The test circuit board was redesigned to include a zero-insertion-force (ZIP) socket to eliminate the need for soldering each package.

Statistical Process Control

A spreadsheet was constructed to allow quick and thorough analysis of the large amount of data that is taken from these devices. Complete diode characteristics, ohmic contact resistances, device input-output resistances, van der Pauw sheet resistance measurements, M-gauge sheet resistance measurements and yield are among some of the data being gathered. This system will aid in device modeling and correlating device performance to specific parameters.

Future Plans

Future plans in the development of the HACT device consist of redesigning the mask set to include test structures on each individual device. The inclusion of characterization diodes and ohmic contact test structures on each device will give a more in depth characterization of each device and permit the determination of material and process uniformity. In addition, future devices will be smaller to improve the transport efficiency. Other changes in the design will improve the wafer yield and enhance the photolithographic steps.

Further optimization of every critical parameter in the HACT device, including ohmic contact resistance, Schottky diode characteristics and yield is planned.

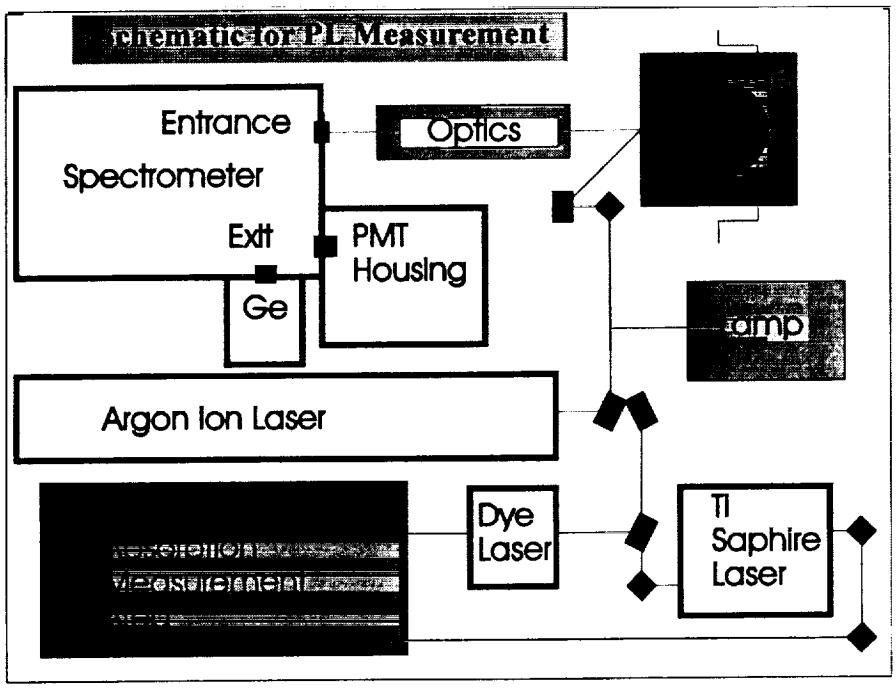
3.3 Testing and Characterization

3.3.1 Optical Characterization of HDTV Material Structures

To support the material growth and processing of devices and to fully characterize compositional quality, optical, structural and electrical properties of AlGaAs/GaAs material and material structures for APD, ACT and CTD improved optical techniques such as photoluminescence and photoreflectance spectroscopies have been set up.

Photoluminescence (PL) experiments can now be performed over a wide range of optical excitation (275nm to 920nm) and sample temperature (4.2K to 300K). In Figure 3.3.1a a schematic diagram of the PL measurement is illustrated. We have used this set up to perform measurements on AlGaAs/GaAs MQW structures at low temperatures. Figure 3.3.1b shows an experimental PL spectrum as a function of energy for such a structure.

a)



b)

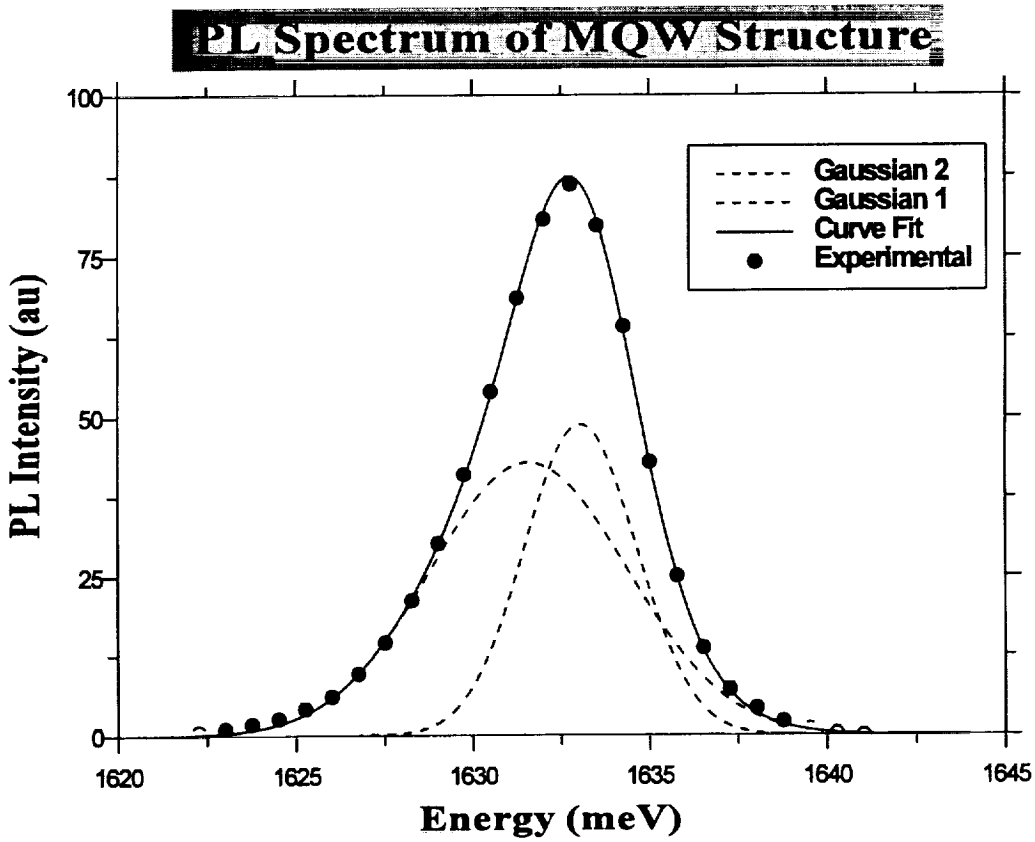


Figure 3.3.1 Schematic of a) photoluminescence system and b) experimental and theoretical PL spectra from GaAs/AlGaAs MQW sample.

Also shown are the synthesized curves that effectively identify features not readily seen by the measurement. Specifically they indicate that the experimental PL spectrum is actually composed of emissions from two quantum wells whose widths are within one monolayer of each other. From this spectrum we obtain information concerning crystalline quality, shallow donor and acceptor levels, alloy composition as well as the width of quantum wells and interface smoothness at the heterointerface.

We also employ photoreflectance (PR) for precise determination of alloy composition, band edge impurities and doping. This technique is readily applicable to process control because it can easily be done at room temperature and above. Figure 3.3.2a illustrates the typical setup for PR measurement and Figure 3.3.2b shows a room temperature PR spectrum of a GaAs sample along with its synthesized curve.

To determine uniformity of material properties across wafer we have developed a Surface Uniformity Scanning technique in which the PL measurement is repeatedly performed across the entire sample. Fig 3.3.3 shows the results obtained from a series of 15 PL scans taken across the wafer as a function of wavelength. The percentage change in peak's location is a direct indication of sample uniformity. This information can be used to feedback to modeling, growth and other processing activities.

Currently we are working on plans to implement the Surface Uniformity Scan using PR. Because this measurement can easily be performed at room temperature, PR could be used as an in-situ/online optical monitor of growth and device fabrication.

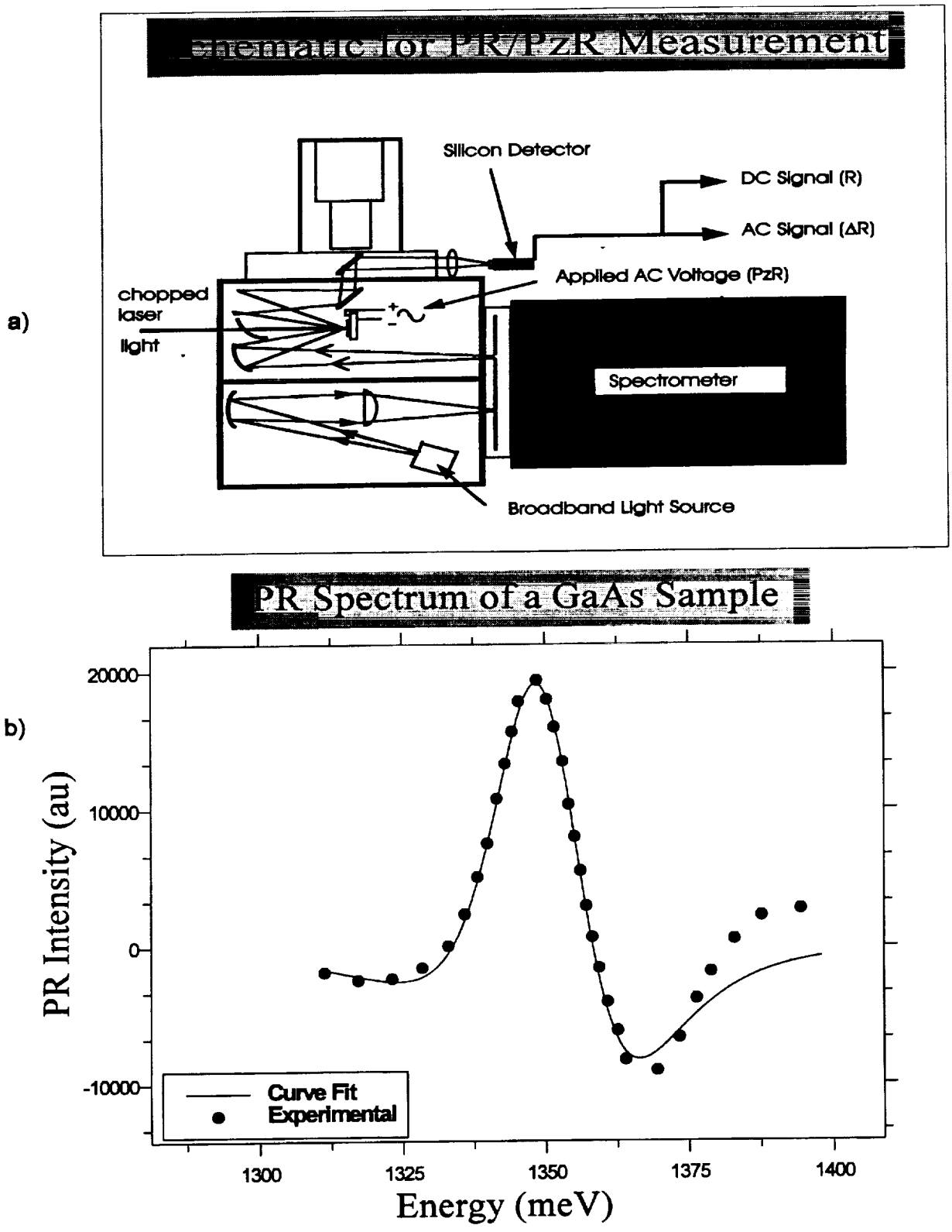
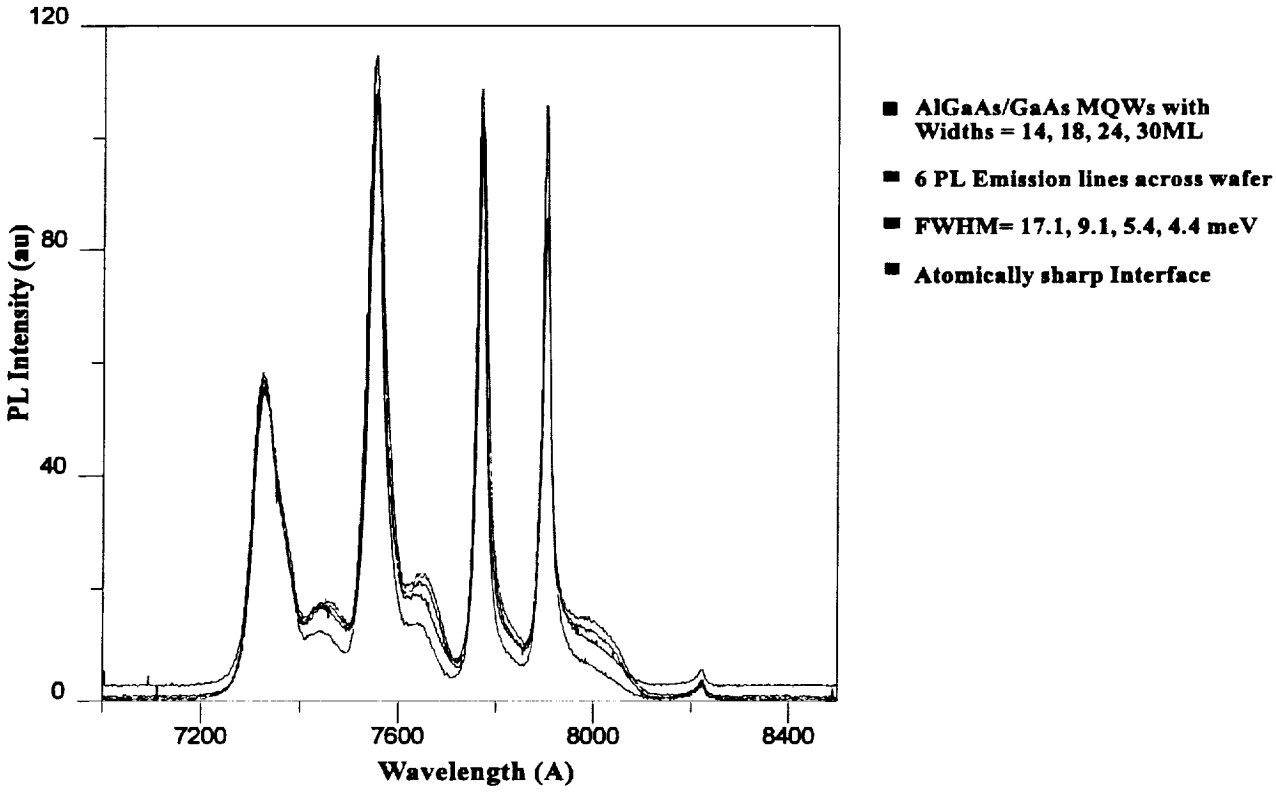


Figure 3.3.2 Schematic of a) photoreflectance/piezoreflectance system and b) room temperature experimental and theoretical PR spectra from GaAs sample.



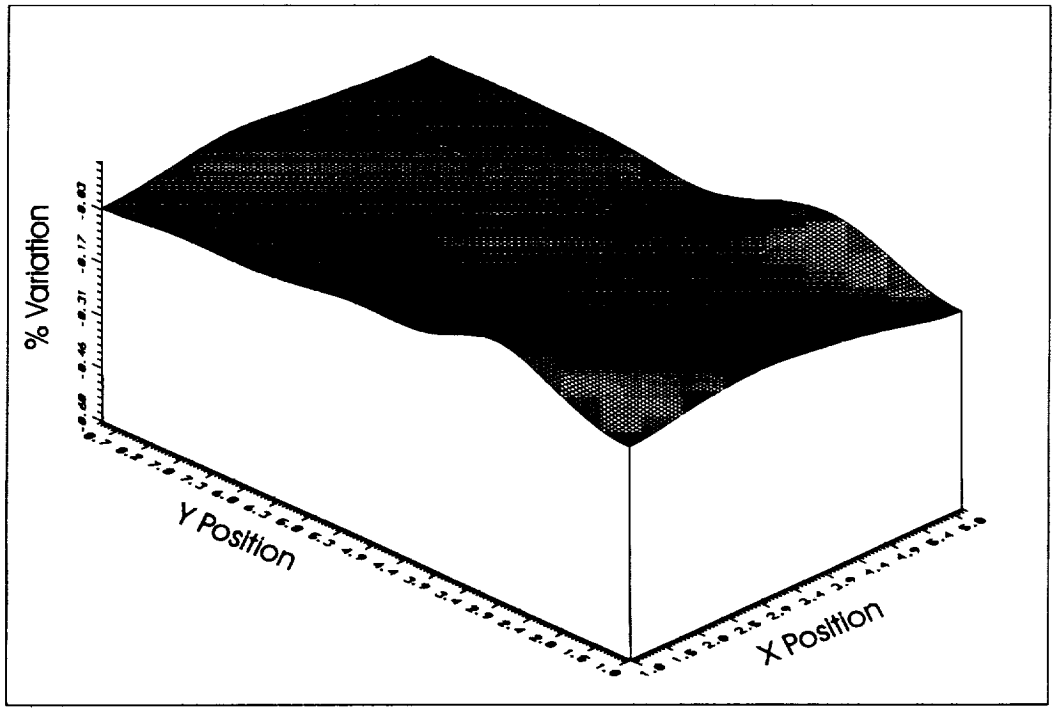


Figure 3.3.3 Pl spectra taken from 15 different locations on a GaAs/AlGaAs MQW sample and a surface uniformity plot of peak wavelength variation across the wafer.

3.3.2 HDTV Photodiode Characterization

Procedures to fully test and characterize the performance of the Avalanche Photodiode (APD) structures intended for use in HDTV imagers, communications and other applications are being completed. These structures, shown in Figure 3.3.4, consist of a p^+ doped GaAs layer followed by AlGaAs/GaAs Multiple Quantum Well (MQW) grown on an n^+ doped GaAs substrate. The devices are designed and fabricated for pure injection of either electrons or holes (top and backside illumination).

The research capabilities of this lab have also expanded to include various computer automated experiments such as diode spectral response, current-voltage (I-V) and capacitance-voltage (C-V) measurements, as well as photodiode gain and noise measurements all performed in a shielded, low-noise, environment at various temperatures ranging from 10 degrees Kelvin to over 300 K. A brief description of some of the above experiments and the information they provide about the photodiode is presented below. These experiments, coupled with the corresponding theoretical work, provide a complete performance analysis of the HDTV APD's in order to better understand their behavior under various operating conditions.

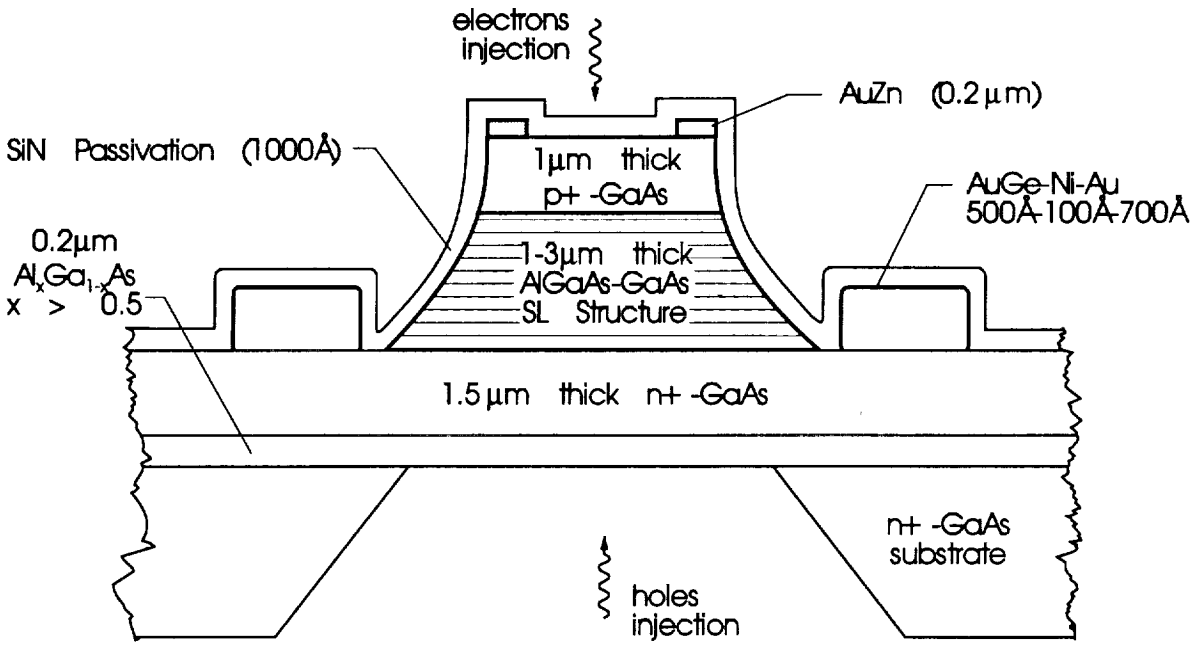


Figure 3.3.4 Cross sectional schematic diagram of GaAs/AlGaAs MQW APD.

Experiment	Description	Information Provided
Spectral Response	Responsivity as a function of wavelength and gain	Sensitivity of photodiode throughout the optical spectrum
I-V response	Diode current output as a function of applied bias (10 K - 373 K)	Photodiode gain and variations with incident light intensities
C-V response	Diode capacitance as a function of applied bias (10 K - 373 K)	Profile of the free charge concentrations in doped APD's
Noise measurement	Noise level as function of laser power density (10 K - 373 K)	Excess noise factor at various diode gain and temperatures

Figures 3.3.5, 3.3.6, and 3.3.7 show some of the results obtained for a typical APD. Figure 3.3.5 shows the spectral sensitivity at zero bias of an APD. In Figure 3.3.6, gain data obtained using IV measurements show the uniformity of the diode gain for different intensities of the laser light. Figure 3.3.7 shows the expected drop in free charge concentration in a doped well APD as a function of temperature. These plots were calculated using data obtained from CV measurements.

There are currently future plans to enhance the capabilities of the above experiments in order to perform more comprehensive measurements such as spectral response uniformity scans across entire APD arrays, and various other tests that would address the manufacturability issues involved in delta-doped avalanche photodiodes.

3.3.3 Charge Transfer and Overflow Device

To evaluate the previously described structures, a flexible DC/transient CTD

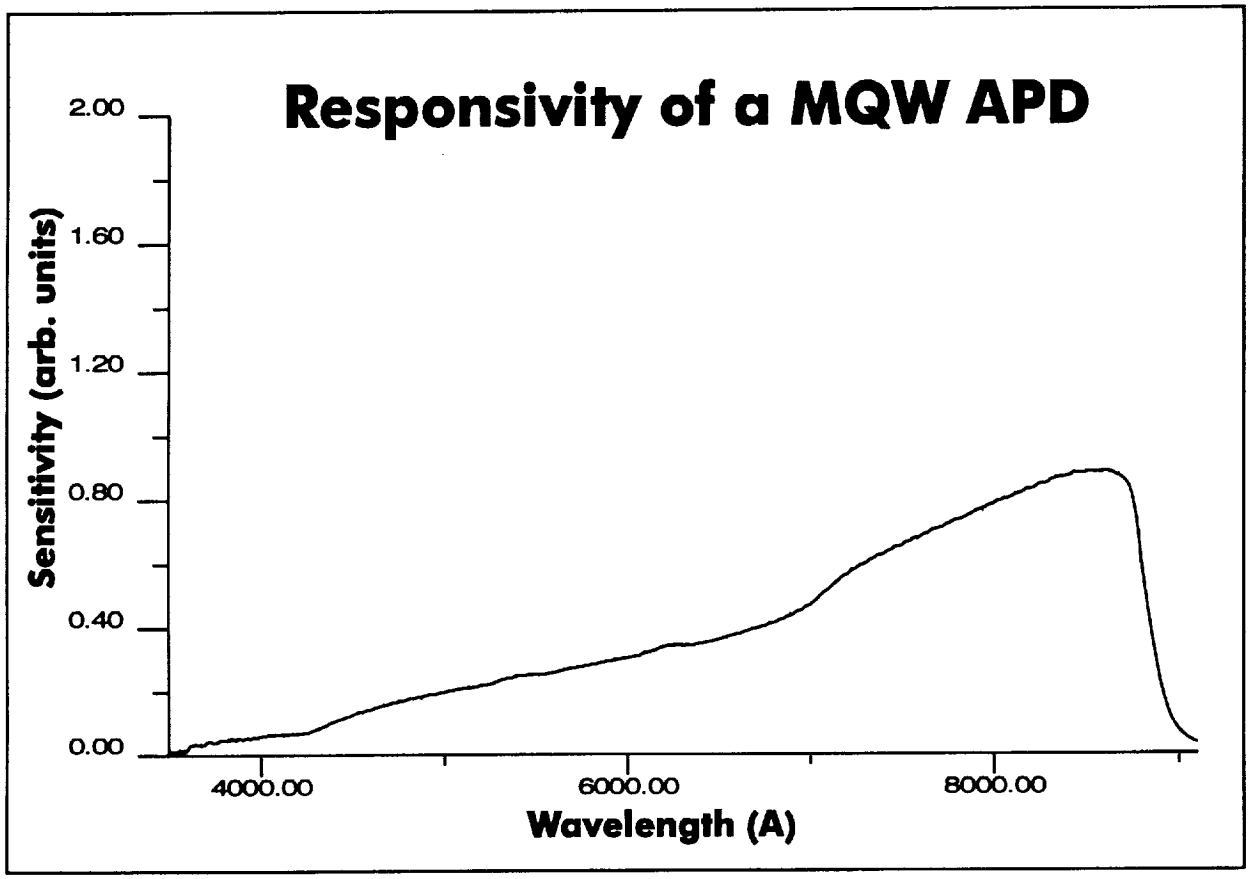


Figure 3.3.5 Room temperature spectral sensitivity of volume doped well APD.

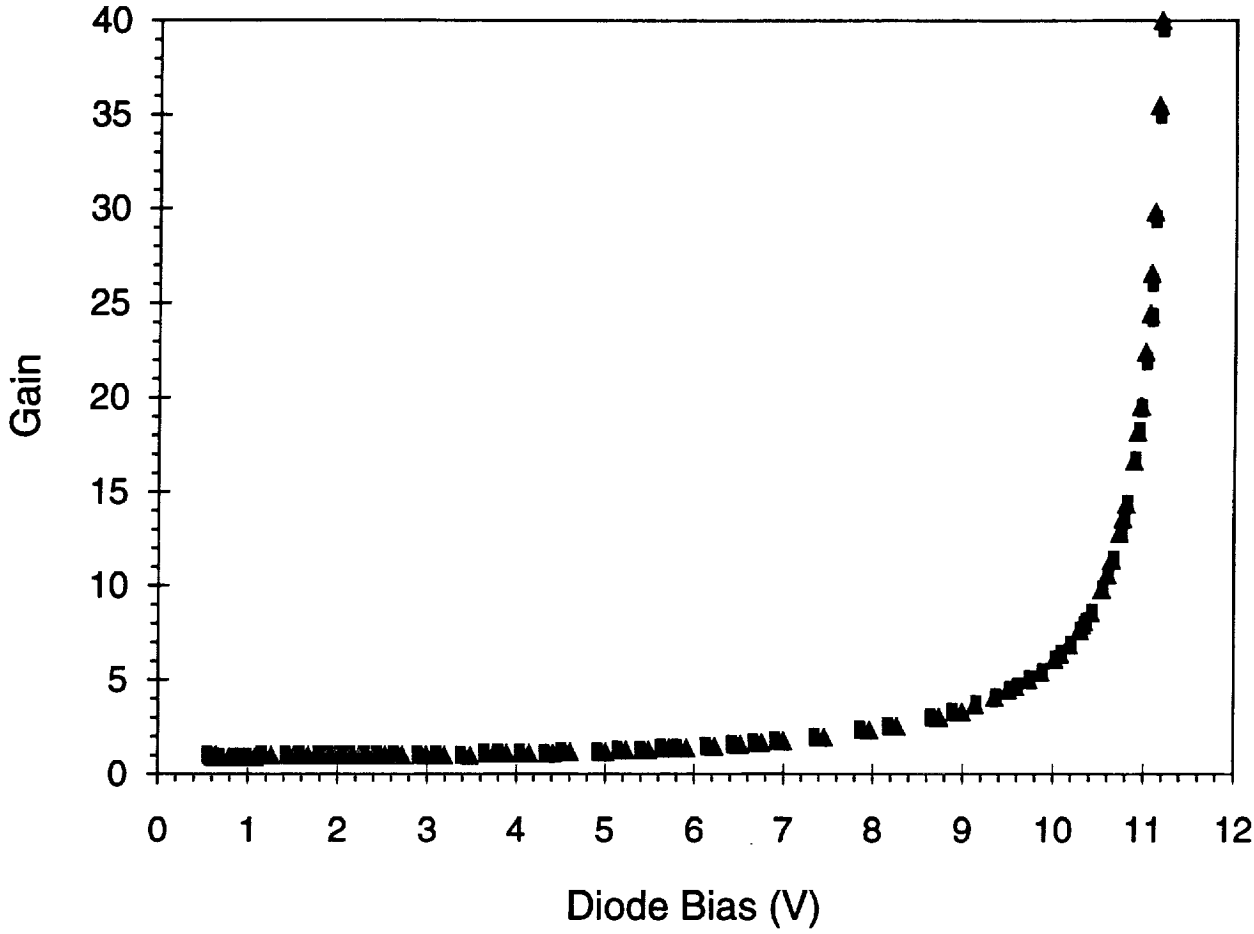


Figure 3.3.6 Gain as a function of applied bias at various light intensities for MQW APD.

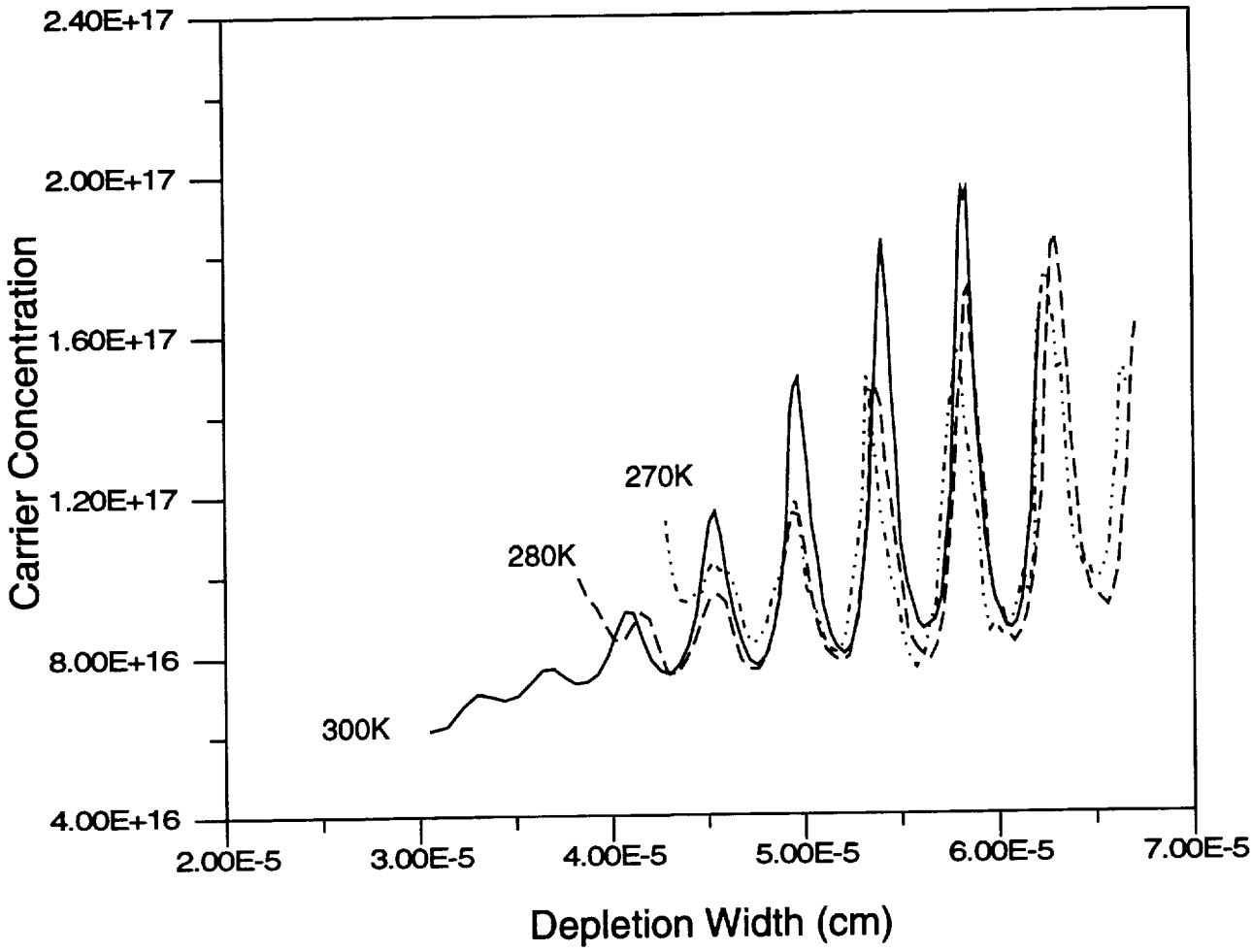


Figure 3.3.7 Net free carrier concentration (determined by C-V measurements) as a function of depth in a doped well APD at various temperatures.

characterization system has been developed and assembled. This system consists of a fast capacitance meter, a pulse generator, an arbitrary waveform generator, a programmable current source and a fast digital oscilloscope, and has the capability of measuring transient voltages and currents from DC to 1 GHz and capacitances with a 10 μs resolution. The system is also able to supply arbitrary voltage waveforms at up to 250 MHz and constant currents to 1 pA. All of these instruments are integrated and computer controlled over a IEEE488 bus allowing data acquisition and analysis to be rapidly accomplished. Figure 3.3.8 shows a schematic diagram of the measurement system. Three CTD devices can be mounted and bonded in a 8-pin DIP package which is placed in a shielded box that has provisions for current sense resistors, shunts and voltage measurement nodes at several locations in the measurement circuit.

Of the three device designs currently under consideration, the volume doped p-type has been fabricated and preliminary results obtained while the delta doped p-type and AlGaAs readout barrier designs have been grown and are in the process of being fabricated.

In the equilibrium conduction band diagrams shown in Figure 3.2.1 for the three readout barrier designs, the arrows indicate the charge flow from the APD to the charge storage well to the ACT readout. It is evident that each design give quite different barrier potentials and also affect the capacity of the charge storage well. The doped barriers present a higher and wider barrier to charge readout. The barrier magnitude and width can be adjusted by varying the concentration and width of the doped region, especially in the case of the delta-doped barrier.

Preliminary results have also been obtained for this design, which in combination with

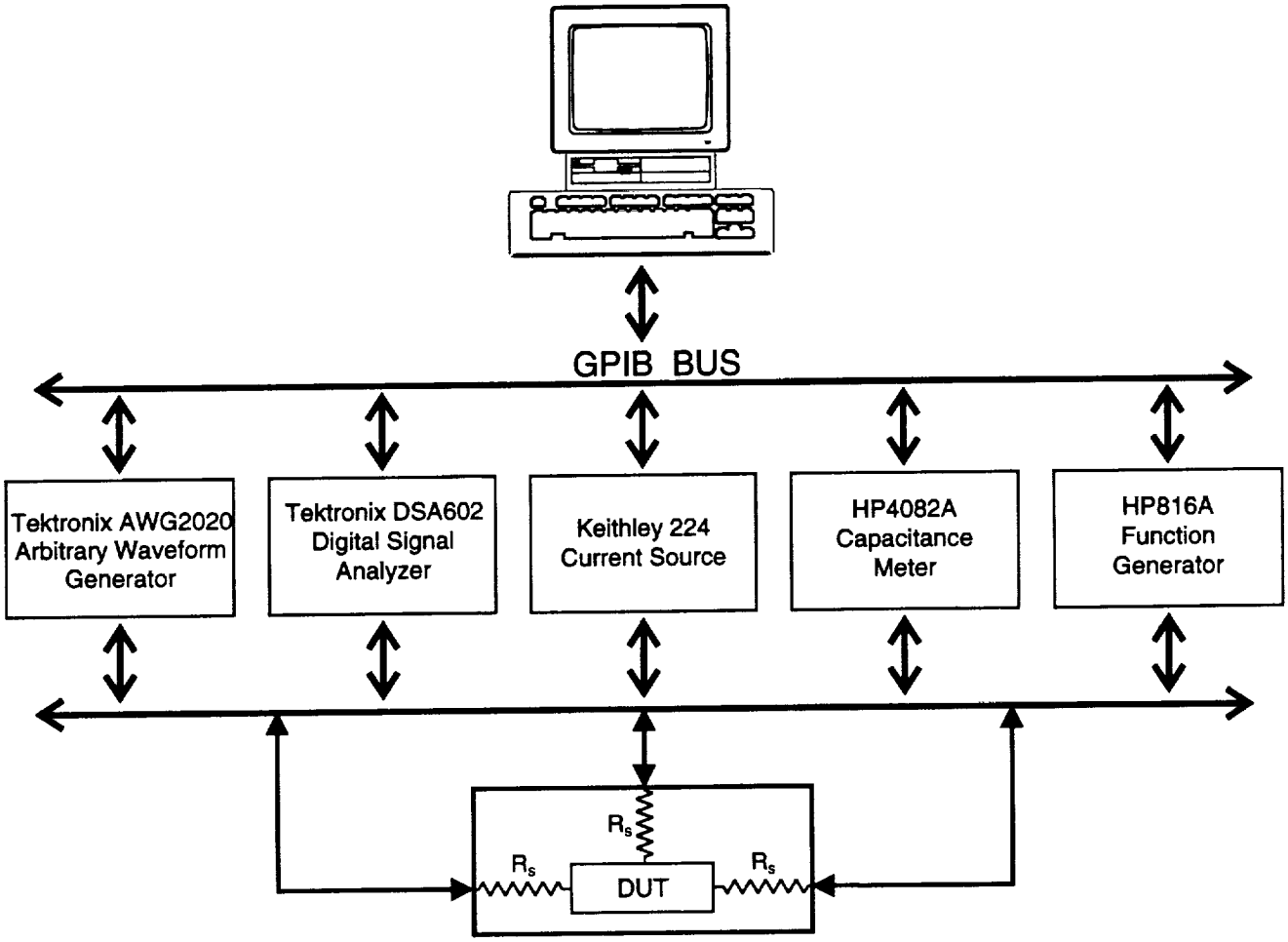


Figure 3.3.8 Schematic layout of CTD fast transient measurement system.

device modeling, indicate that charge transfer is taking place in the charge storage well. Figure 3.3.9 shows the transient capacitance response of a device biased with 5V negative and positive pulses applied to the readout contact. The positive and negative bias pulses cause a reduction in the capacitance of the device due to the removal and filling of electrons in the charge storage well, respectively. The difference between the two results indicate that more charge is being transferred into the well than is being removed. However, the relatively small difference between the two results indicate that the amount of free charge in the well must be reduced. This can be accomplished by simply reducing the doping level in the well. A transient analysis using the hydrodynamic simulator confirms that more charge is injected into the charge storage well as compared to the amount of the existing equilibrium charge concentration that can be removed.

3.3.4 Measurement of HACT Devices

A number of the computer-controlled measurement systems which have been developing for the HACT devices have come on line during the past 6 months. These include DC probe measurements of Schottky barrier diodes and ohmic contacts, HACT I-V characteristics. Soon to be on line are automated facilities for the HACT Frequency Response and the Transient Response. The different tests to be performed on the HACT devices are shown in Figure 3.3.10. Schematics of how some of these test systems are configured are presented in Figures 3.3.11 and 3.3.12. It should be pointed out that our approach to testing is in keeping with the practices of industry, in particular it is in keeping with testing procedures on device assembly and packaging lines. Hence, the software we develop for testing can easily be ported to our industrial partners interested in manufacturing the imager and related

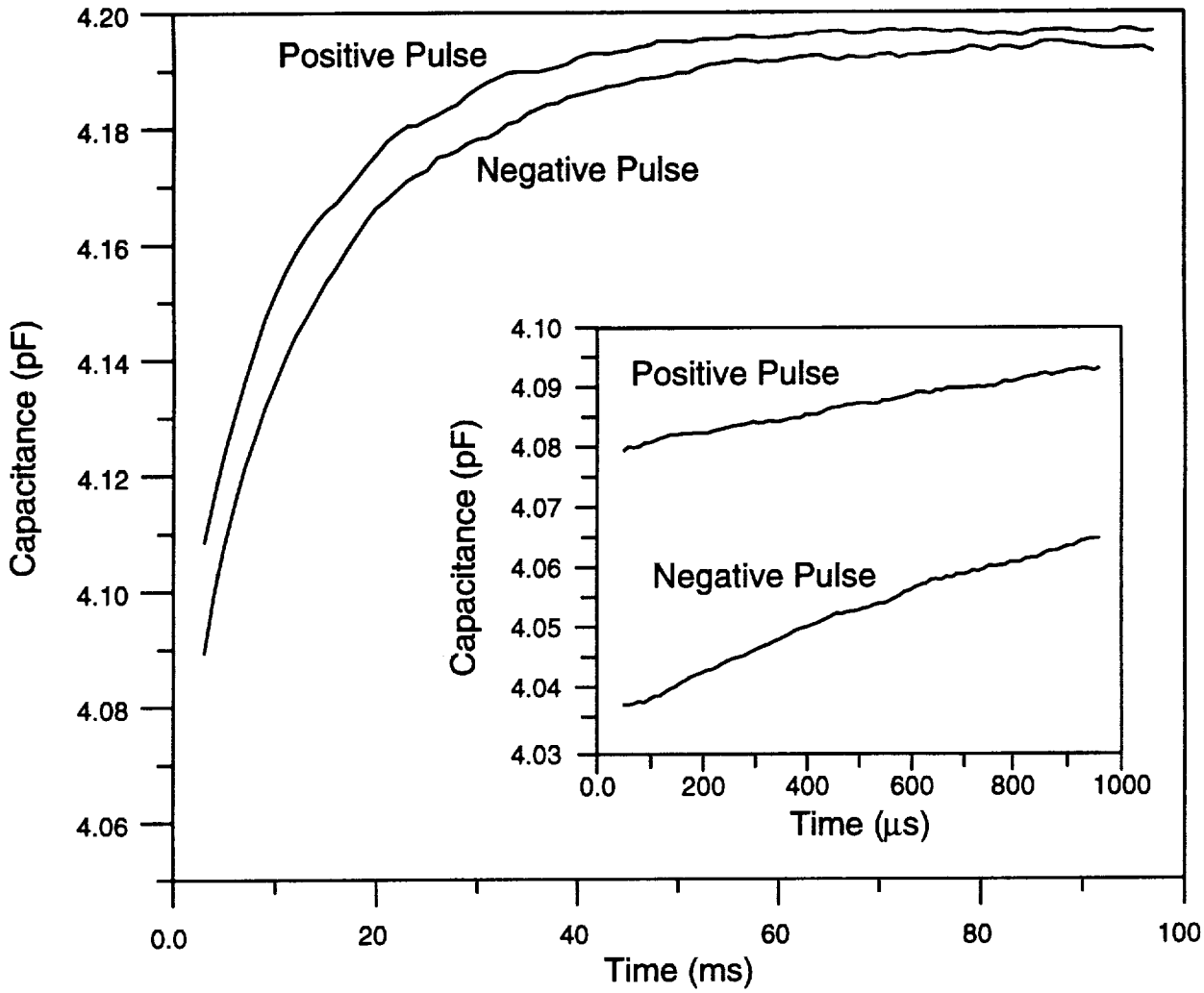
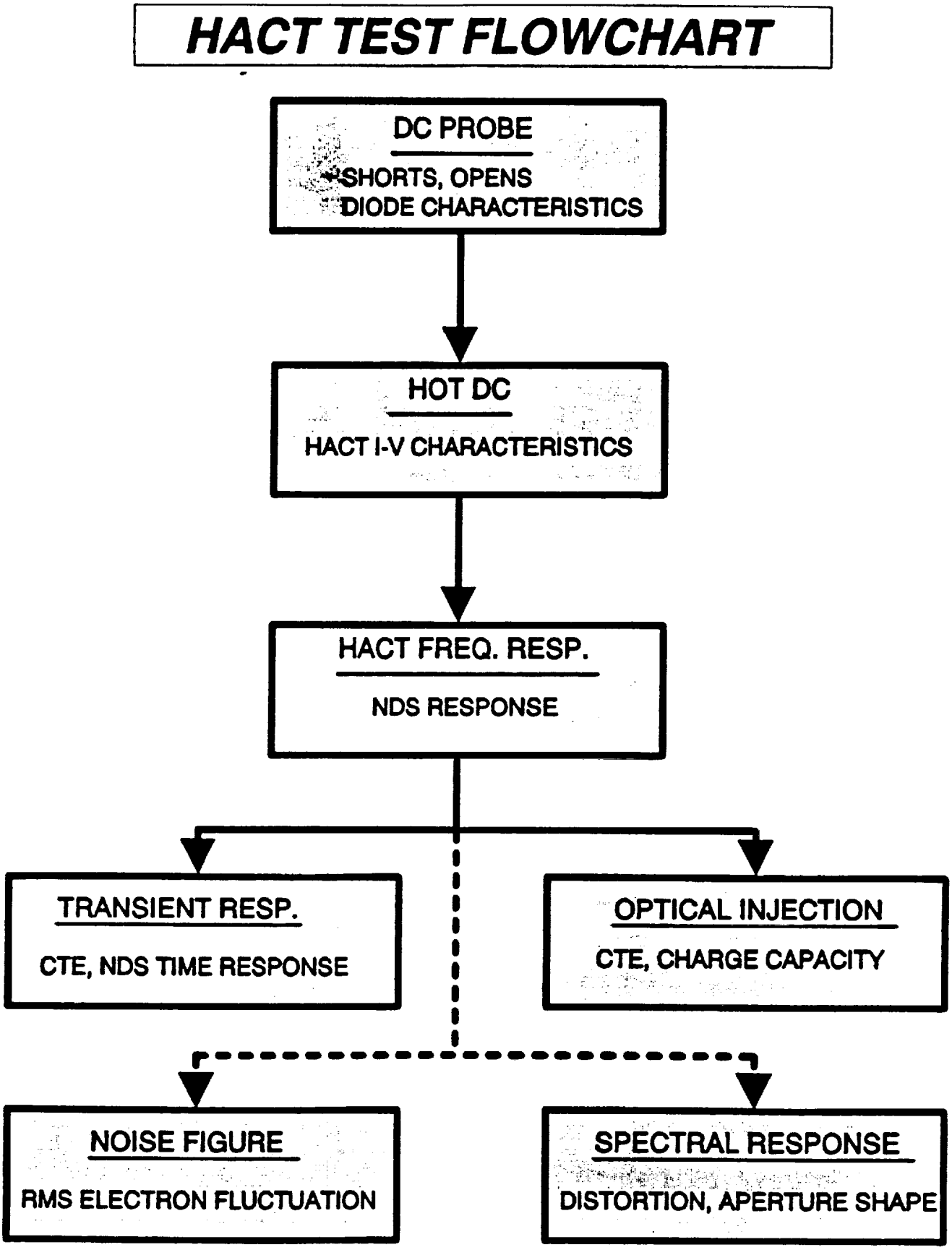
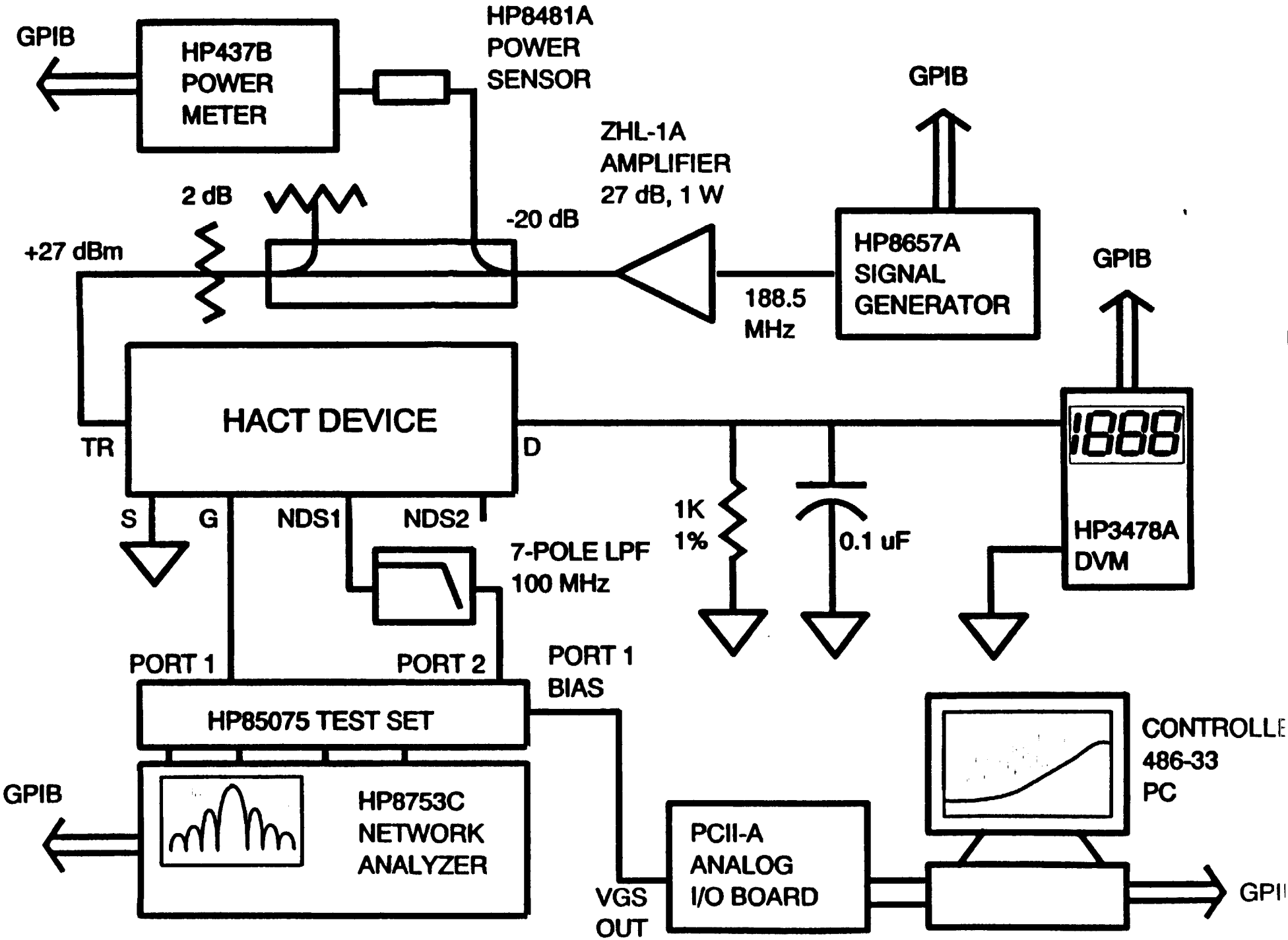


Figure 3.3.9 Transient capacitance response of volume doped barrier CTD to positive and negative 5 V pulses applied to readout contact.

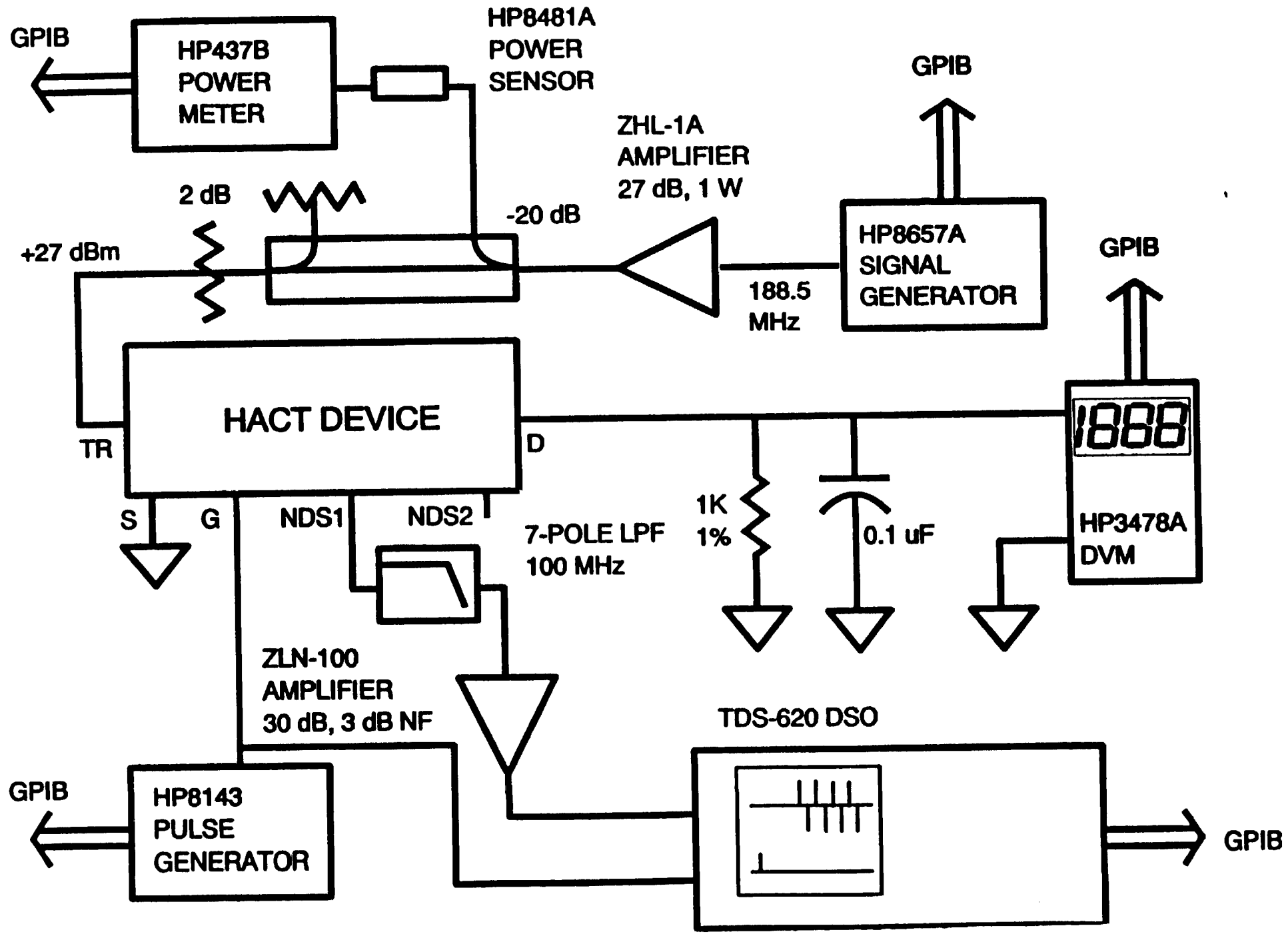


3.3.10 HACT Test Flowchart

HOT DC TEST AND FREQUENCY RESPONSE SETUP



TRANSIENT RESPONSE SETUP



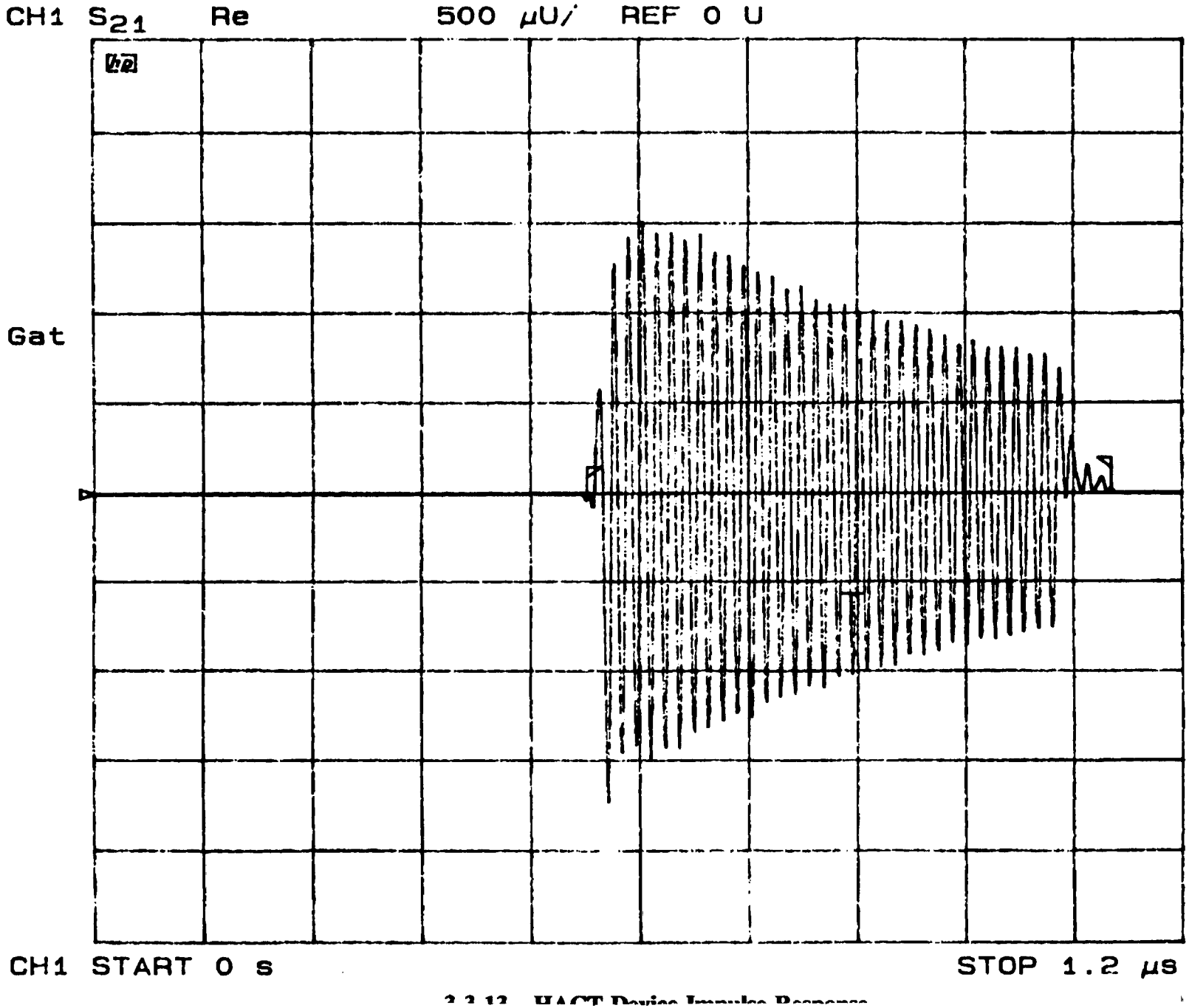
spinoff devices. In Figure 3.3.13 we present the impulse response of HACT device C-3 from wafer lot #1854. The charge transfer efficiency measure on this device was 0.992 and the measurement of this device and others has indicated that our ACT device architecture needs to be improved. Several alternative approaches are being considered and will be explored experimentally within the next few months.

3.3.4.1 Experimental Acoustic Studies

The breakout of the experimental acoustic portion of the program is presented in Figure 3.3.14. In the conduct of our work we design, fabricate and test SAW devices on GaAs-based structures. The testing includes the measurement of the SAW propagation characteristics in various structures *via* our knife-edge laser probe system. This experimental setup is under computer control and allows us to measure the magnitude and phase of the SAW throughout the device. This data in turn enables us to extract such important features as the piezoelectric coupling coefficient, SAW velocity, attenuation and the slowness surface. Among the important work completed within the last six month period was the completion of the measurements of piezoelectric ZnO films on GaAs and the further measurements of SAW waveguides and our ability to accurately predict beam profiles in said structures using Stack Matrix theory.

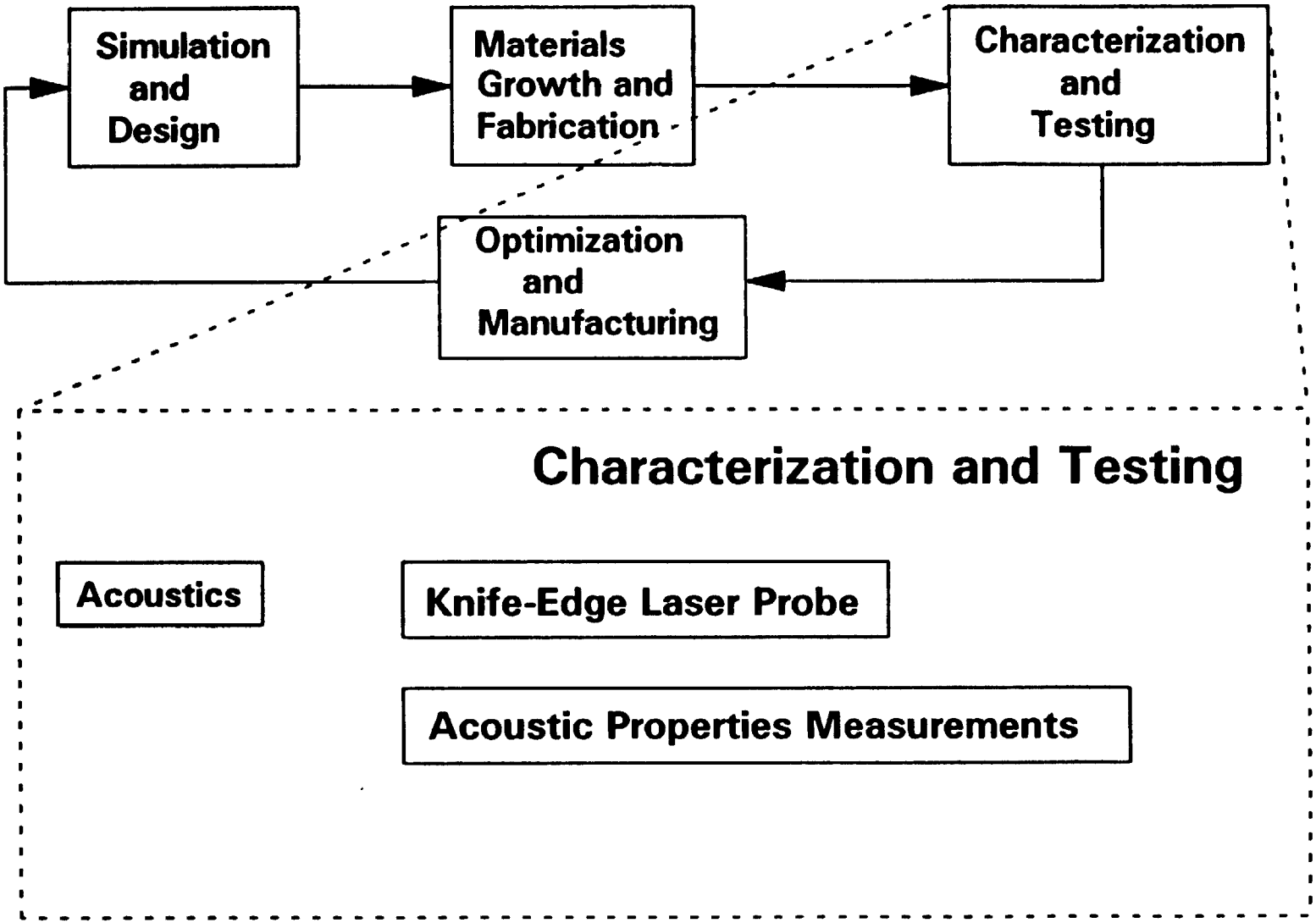
A comprehensive experiment on the acoustic and piezoelectric properties of ZnO films on GaAs was completed. This included sputtering these films at Motorola; design, fabrication and testing of surface acoustic wave (SAW) devices at Georgia Tech; and a line-focused-beam acoustic microscope measurement of the SAW properties at the National

Impulse Response of a
64-TAP HACT Delay Line
CTE = 0.992



Wafer Lot 1854
Device C-3
P_{SAW} = +27 dBm
I_C = 9.8 µA
f_{SAW} = 188.5 MHz

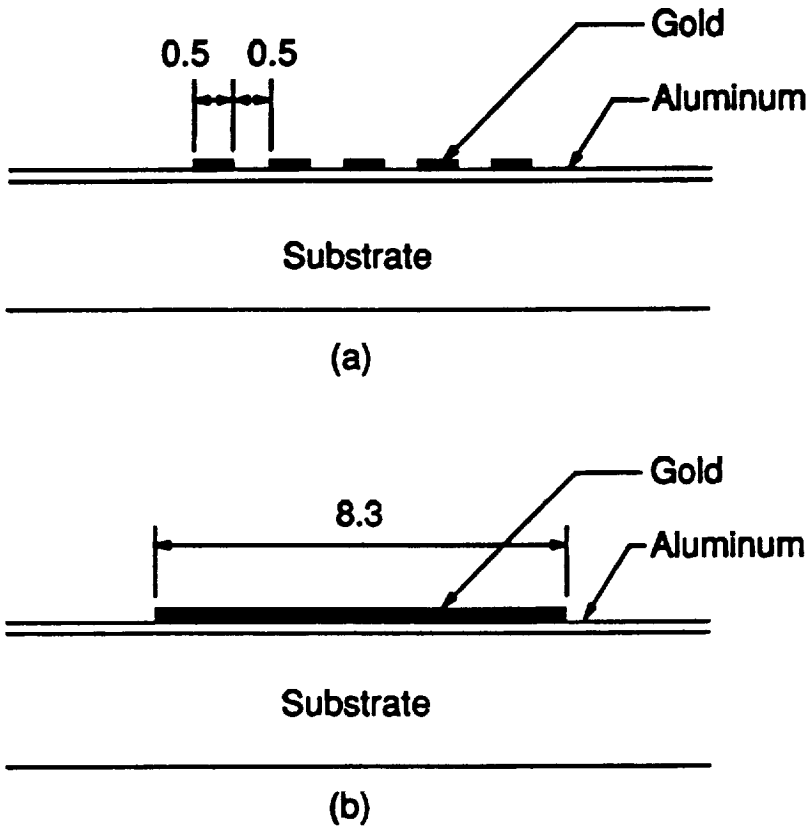
3.3.13 HACT Device Impulse Response



3.3.14 Characterization and Testing: Acoustic Studies

Research Council of Canada. In comparison with bare GaAs, a 10X increase in the piezoelectric coupling was achieved at a modest cost of 0.6 dB/μsec of acoustic propagation loss. One implication of this is that an ACT device with a ZnO film overlay would operate with 13dBm of RF drive power to the SAW transducer instead of the 28dBm required with current architectures. This potential for a 15dB reduction in the RF drive power is very significant and would make ACT devices so designed more attractive for microwave radio telecommunications and other applications where there are where there is a relatively strict power budget. In addition, this reduction of power would increase device lifetime. Among the findings of this study are that the smaller the ZnO grain size, the better the quality of the film and by this we mean that the piezoelectric coupling coefficient and the attenuation approaches that which would be expected of single crystal ZnO. In our case the best films were DC Triode sputtered. It was also clear that it was important to have a thin-film dielectric between the GaAs substrate and the ZnO film to prevent Zn doping of the substrate during sputtering. This doping is manifested acoustically as an increase in the SAW attenuation. An interesting result was that the presence of the ZnO film alters the slowness surface of the aggregate structure. For GaAs alone the slowness surface is concave upward indicating that the SAW beam emerging from an interdigitated transducer will focus before finally spreading outward. With the addition of the ZnO film the slowness surface becomes concave downward and hence the SAW beam tends to diffract more quickly. This particular acoustic aspect of the structure is still under study. A further implication of this work is the prospect of SAW filters monolithically integrated with GaAs electronics.

A schematic illustration of some of the waveguide structures is shown in Figure 3.3.15



Schematic illustration of the cross section of (a) multichannel and (b) single channel waveguide on ZnO/GaAs

3.3.15 Schematic illustration of the cross section of (a) multichannel and (b) single channel waveguide on ZnO/GaAs

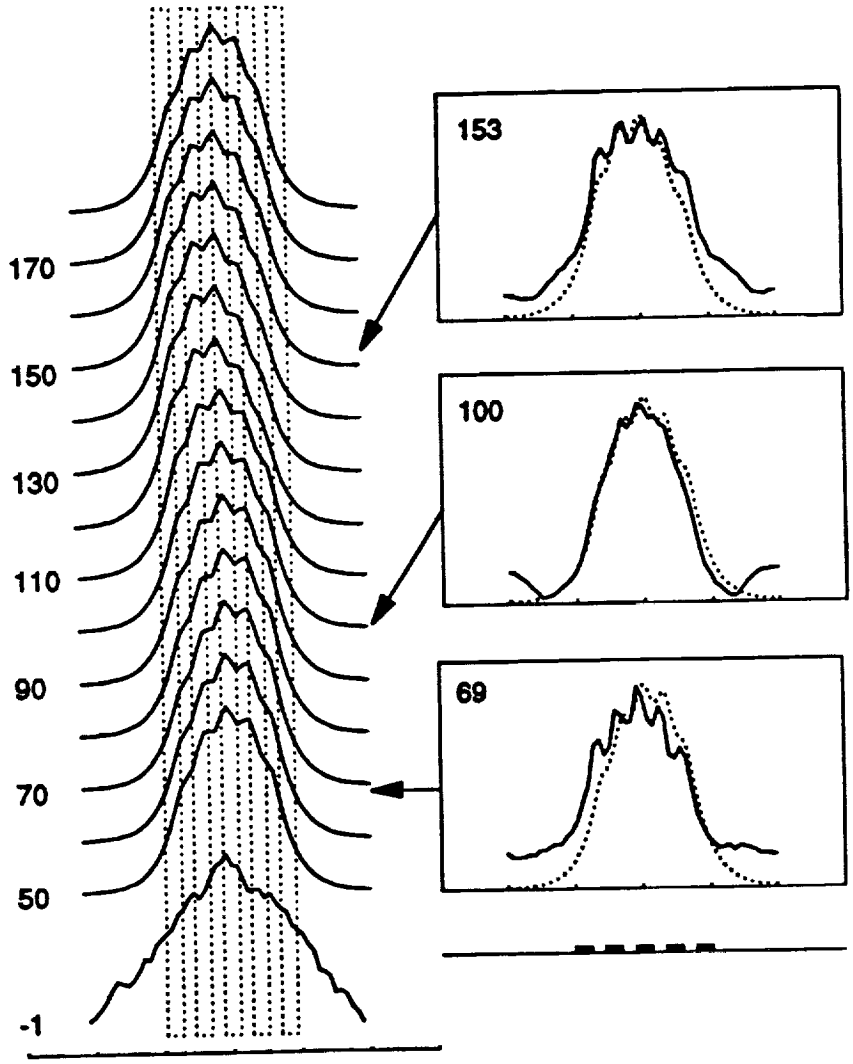
and the resulting laser probe measurements of the mode profiles are shown in Figure 3.3.16. The predicted profiles closely resemble the measured ones though there is some discrepancy due to inaccuracies in the value we use for the acoustic velocity in the different regions of the waveguide and in our ability to predict the beam profile as it propagates given an arbitrary beam profile at the entrance to the waveguide. This too will be improved in the coming months.

3.4 Design for Manufacturability

Very recently Professor Gary S. May has joined our team and has initiated work on issues related to manufacturability. The breakout from the overall project block diagram for this Optimization and Manufacturing task is shown in Figure 3.4.1. Already this work has resulted in a publication [16] and is well underway. By including these manufacturing considerations early in the development of the HDTV chip we will be able to make design choices that ensure high yields for the chips in an industrial environment. The first manufacturability study we performed was the study of the impact of defect density on the yield of ACT transversal filters. Current work is underway to look at the lifetime of APDs. Future work will include knowledge of the human visual system and its impact on fault tolerance in the APD array.

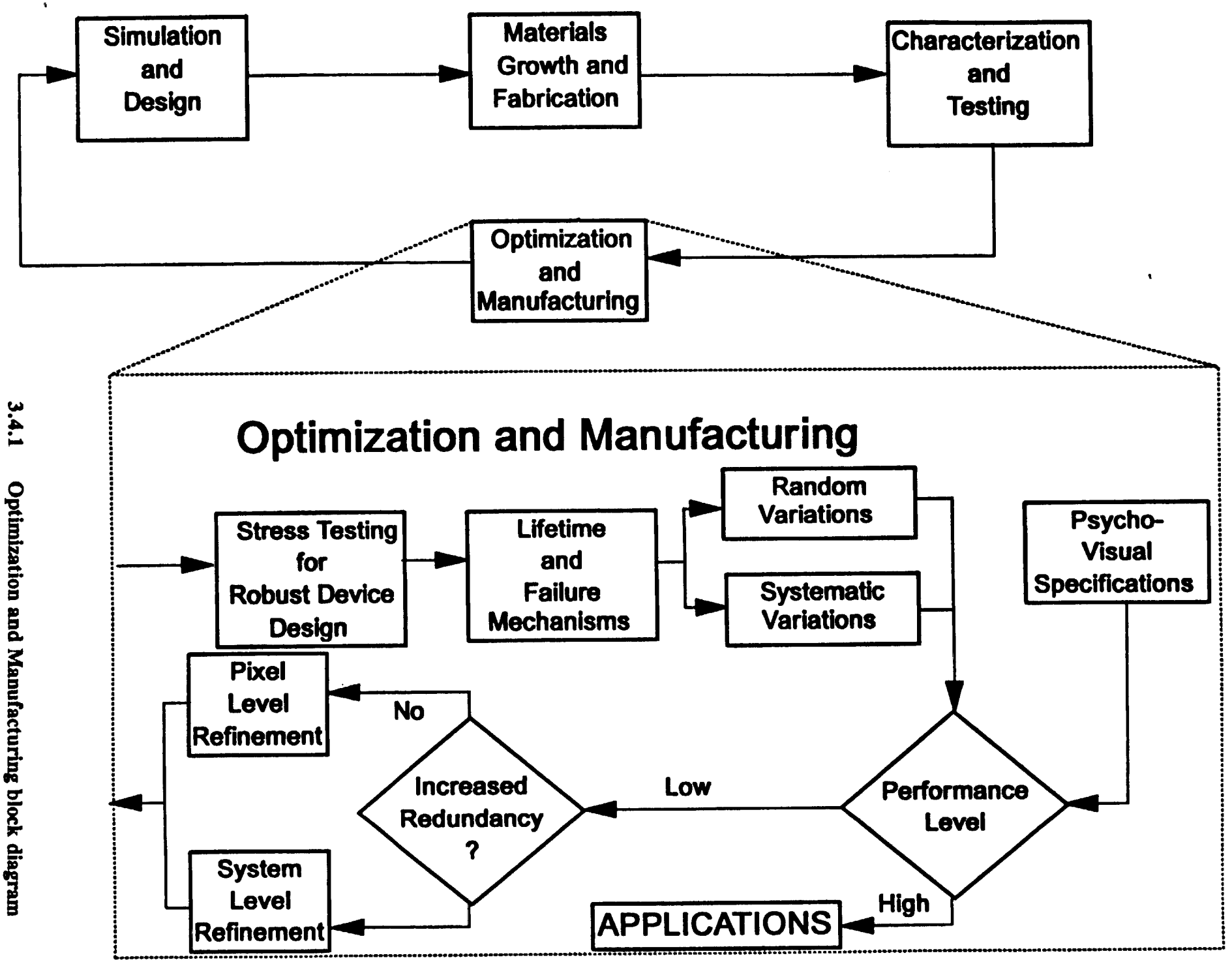
4. 0 Interactions

An integral part of the project is to develop close ties to industry to facilitate technology transition. Though the overall goal of the program is to develop a high definition systems



Predicted and measured beam profiles in multichannel waveguide.

3.3.16 Predicted and measured beam profiles in a multichannel waveguide



3.4.1 Optimization and Manufacturing block diagram

imaging chip, other technical advancements produced in this program may be successfully exploited commercially. In this section of this report, we review our progress in fostering external ties to both industry and government laboratories.

4.1 Technology Transition

The stack matrix theory developed for SAW waveguide analysis and discussed in Section 3.1 is being used as a design tool by a group at Bell Northern Research headed by Dr. John Saw. Additional industrial users of this design tool and the coordinating research director within that company are SAWTEK (Brent Horine), RF Monolithics (Dr. Ben Abbot), and Siemens (Dr. Clemens Ruppel).

A simplified version of our advanced hydrodynamic device simulator has been developed to study the performance of interdigitated photoconductors. This research has been supported by the Digital Equipment Corp. for the past two years. Due to financial hardships at DEC, this program has been temporarily suspended, however we are continuing a dialog with DEC towards restarting this project. It is expected that our design tool will ultimately be transferee to DEC for use in their optical design group. Nevertheless, the simplified design tool has been completed and we are continuing our study of interdigitated photoconductors with the hopes that DEC will restart support for the theoretical group.

Bell Northern Research has contracted with Dr. Brennan's group to evaluate the performance of APD devices. This program has several goals. The first is to use the theoretical tools described in Section 3.1 to aid in the understanding and optimization of a commercial InP based separate absorption, separate multiplication APD that BNR

manufactures. The second focus of the BNR work is to use the advanced theory of impact ionization along with the ensemble Monte Carlo code to study the performance of novel GaInAs/AlInAs based APDs for potential use in lightwave communications systems. Finally, BNR would like to obtain an improved version of our hydrodynamic simulator sor use in developing APDs in their laboratory. Therefore, it is expected that an executable version of our hydrodynamic simulator including a state-of-the-art formulation of the impact ionization rate will ultimately be delivered to BNR for use in their lab.

BNR has also contracted with Dr. Hunt's group to investigate the development of ACT devices for various applications. Additionally, BNR has sent a professional employee, Mr. Tom Cameron, to work towards his Ph.D. degree with Dr. Hunt. In this way, expertise in ACT technology will be effectively transfered to BNR.

4.2 Collaborations

As described above, Bell Northern Research, BNR, is a major collaborator in this project. In addition to financial assistance, BNR has also committed personnel as evidenced by their support of Mr. Tom Cameron as a Ph.D. student in the program. In return, BNR anticipates a technology transfer from the Georgia Tech team to aid their commercial products, primarily their ACT and APD devices. As an outgrowth of the BNR interaction, a strong collaboration with the National Research Council of Canada has been forged. Some experimental expertise has been provided by the National Research Council of Canada which has and presumably will greatly foment progress on the imager. Additionally, discussions with Motorola have commenced with the aim of fostering a collaboration with Motorola.

Already, we have obtained samples from Motorola and are trying to augment our existing ties.

We have approached two national laboratories, Los Alamos National Laboratory and Sandia National Laboratory, for technical assistance in this project. Dr. Brennan visited Los Alamos in July, 1993 to discuss collaborations involving parallel computing. Specifically, it was suggested that a Ph.D. student of Dr. Brennan's, Mr. Joe Parks, spend some of his time at Los Alamos studying how our hydrodynamic simulator and Monte Carlo codes can be ported onto the CM5 supercomputer. The specifics of this arrangement still need to be clarified and Mr. Parks needs to finish his classwork before this segment of the collaboration can commence. Nevertheless, Dr. Brennan has been invited by Los Alamos to return to the labs in Winter 1994. Both Drs. Brennan and Summers visited Sandia Labs in July 1993 to discuss possible collaborations with Sandia. Specifically, we seek Sandia's assistance in improving the ion implantation process used in the CTD designs. Sandia has a long history of excellence in compound semiconductor technology and has the resources to do a thorough study to improve ion implantation in GaAs. This is a crucial technology which does not exist at Georgia Tech and as such requires outside assistance. It is expected that Drs. Brennan and Summers will return to Sandia to finalize the collaboration before the end of 1993.

Finally, we are beginning work with Dr. Bill Glenn at Florida Atlantic University. Dr. Glenn is an expert on psycho-visual relationships. With Dr. Glenn's added expertise, we will be able to refine the imaging chip design to ensure that it will be suitable for commercial applications.

5.0 Future Plans

The primary focus of the project in the next year will be to refine the design and optimize each of the component devices in the imager chip, the ACT, CTD and APD. Additionally, work will progress towards the integration of each of the separate components into a cohesive unit. Specifically, we plan to develop a small, one-dimensional prototype array in the next 12 -18 months. A short list of the goals and steps that we will take to these ends in the next year of the project is as follows:

1. Final acquisition of key personnel in the various aspects of the program. Due to a delay of 6 months in transfer of funds to Georgia Tech we have experienced a delay in hiring new personnel. We plan to hire additional professionals to aid in materials growth and fabrication.

2. Theoretical and experimental analysis of alternative ACT and CTD device geometries aimed at increasing the charge capacity, transfer efficiency and manufacturabity. Specifically, we will examine alternative ACT structures which include a p-type top layer for surface state control and lateral transfer CTD devices to simplify the device and enhance its reproducibility.

3. Integration of ZnO films with ACT devices.

4. Integration of APDs and ACTs to make a linear array.

5. Revision of the hydrodynamic simulator for APD device simulation incorporating the interband impact ionization rate results derived from the Monte Carlo model.

6. Investigation of ion implantation in GaAs/AlGaAs heterostructures in collaboration with Sandia National Labs.

7. Experimental evaluation of delta-doped APDs.

8. Lifetime testing of the APDs.

9. Refinement of the electron and hole Monte Carlo simulators to determine the optimum operating characteristics of the delta and volume doped APD structures.

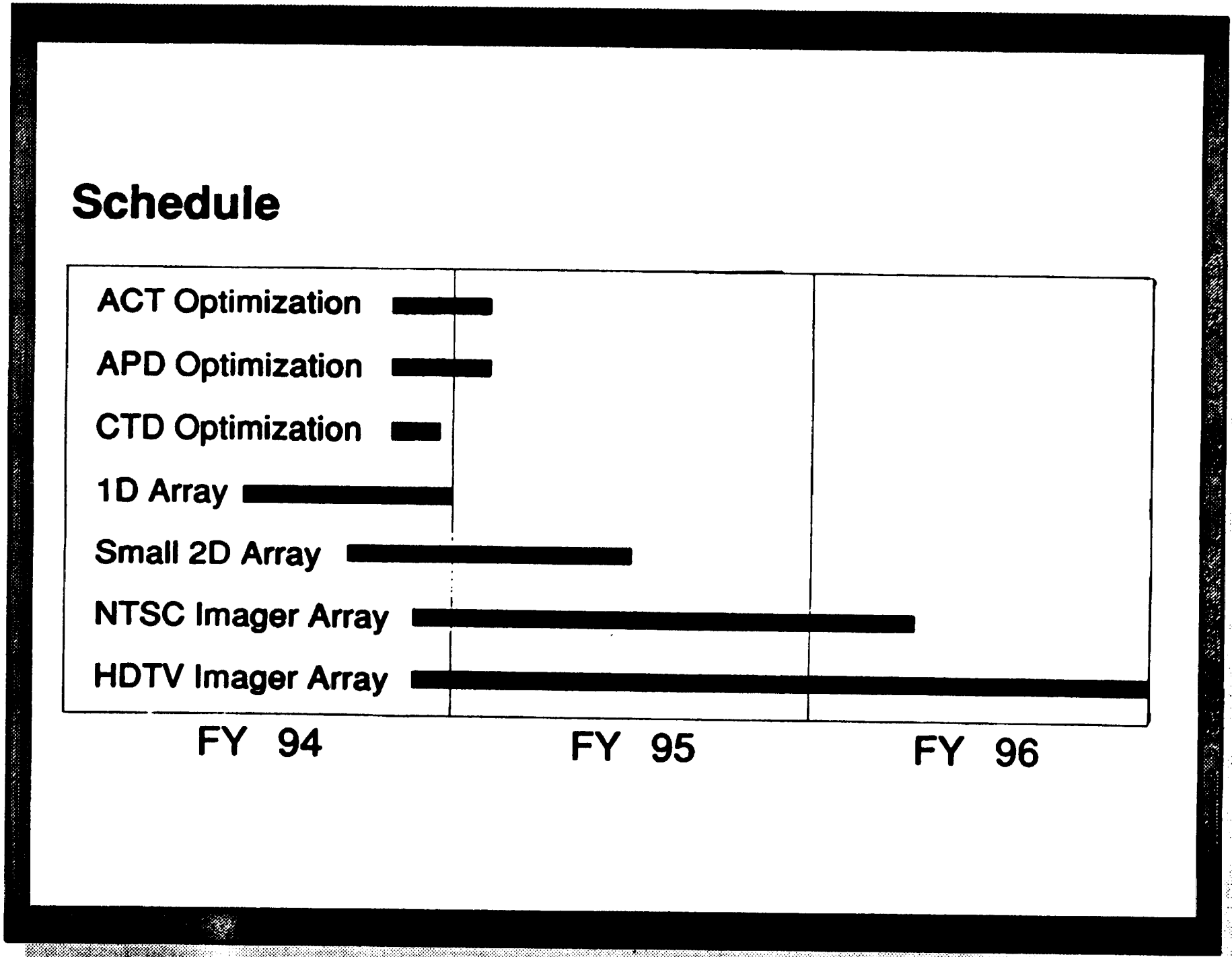


Figure 5.1: Schedule for the HDTV program showing goals through the next three fiscal

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	9/30/93	Semiannual 1 Apr 93 - 30 Sept 93

4. TITLE AND SUBTITLE

"An Acoustic Charge Transport Imager for High Definition Television Applications"

5. FUNDING NUMBERS

NASA Grant #NAGW-2753

6. AUTHOR(S)

Dr. William D. Hunt
Dr. Kevin F. Brennan
Dr. Christopher J. Summers

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

School of Electrical and Computer Engineering
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

8. PERFORMING ORGANIZATION REPORT NUMBER

E21-687 and E21-H83

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

NASA Headquarters
Code PT
Washington, DC 20546
Attn: Thomas J. Bentsen

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

NASA Grant #NAGW-2753

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

1) Invention of a new, ultra-low noise, low operating voltage APD which is expected to offer far better performance than the existing volume doped APD device. 2) Performance of a comprehensive series of experiments on the acoustic and piezoelectric properties of ZnO films sputtered on GaAs which can possibly lead to a decrease in the required rf drive power for ACT devices by 15dB. 3) Development of an advanced, hydrodynamic, macroscopic simulator used for evaluating the performance of ACT and CTD devices and aiding in the development of the next generation of devices. 4) Experimental development of CTD devices which utilize a p-doped top barrier demonstrating charge storage capacity and low leakage currents. 5) Refinements in materials growth techniques and insitu controls to lower surface defect densities to record levels as well as increase material uniformity and quality.

14. SUBJECT TERMS

15. NUMBER OF PAGES
82

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	Unlimited